

# INSTRUCTION MANUAL CONTENTS

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## INTRODUCTION

### GENERAL

The IBM Magnetic Tape "Selectric" Composer consists of four basic units. These four basic units are:

1. Magnetic Tape Reader — Model 6310
2. Composer Control Unit (CCU) — Model 6320
3. Translator
4. Modified IBM "Selectric" Composer

The Magnetic Tape Reader contains a modified version of the tape deck used on the Model IV MT/ST. The circuit-breaker and back-stepping mechanisms have been removed, and the deck has been re-wired to meet the application requirements of the MT/SC.

The unit is housed in a standard MT/ST cabinet. The control panel contains Load and Unload keybuttons for both the right and the left stations, a Skip keybutton, a Search keybutton, and a Reread keybutton. A single Cover Unlock keybutton unlocks either tape cover provided the tape has been unloaded on that station. No reference dial or window is provided because the MT Reader always searches forward one reference code for each depression of the Search keybutton. A more detailed description of the keybutton functions may be found in the Tape Reader section.

The Composer Control Unit (CCU) accepts input from a tape reader or the keyboard and automatically calculates solutions for justified, centered, flush left, flush right and leadered copy. The CCU is mounted in the main console desk which also houses the Translator and modified Composer. The CCU is composed of 34 SLT/SLD cards mounted in a logic board, a core storage memory and a power supply. The logic is divided into Input interface logic, Calculating logic, Memory logic and Output interface logic. A keyboard mounted on the desk allows the operator to enter set-up and tape control information into the CCU. The keyboard also contains test switches, available only to the Customer Engineer, which may be used for troubleshooting.

The Translator unit is an electro-mechanical device used to convert the electronic signals generated by the CCU to mechanical energy to operate the Composer keylevers. The Translator uses 8 magnet assemblies for proper character selection plus a magnet for activating its cycle clutch. A 1/35 H.P. motor drives the mechanism. As the various magnets are energized, their armatures are attracted to release an associated permutation bar. The permutation bars allow one seeker to supply a pull on the keylever link through an operating arm. A Composer operation results.

The output device for the MT/SC is a standard Composer modified with additional hardware for automatic output. Keylever links have been added to the character and functional keylevers. Two photo-cells are attached for feedback purposes in order to time the electronics in the CCU to the mechanical speed of the modified Composer.

A Paper Tape Reader is also available for input to the CCU. This unit is a modified version of the Model 1054 PT Reader. The reverse stepping mechanism is not used and the tape guides have been positioned to read 6 or 8 channel, advanced feed-hole, chad type tape, punched to graphics industry standards. Only one additional SLT/SLD card is required to match the PT Reader to the CCU input interface. The Paper Tape Reader may be used as sole input for the CCU or used in conjunction with the Magnetic Tape input. However, both PT and MT input cannot be used simultaneously. The numerical designation of the modified Paper Tape Reader is Model 6354.

### SPECIFICATIONS

#### SHIPPING WEIGHTS (APPROX.)

UNIT	PADDED VAN	COMMON CARRIER
IBM "Selectric" Composer (Modified)	65 Lbs.	65 Lbs.
Composer Console	207 Lbs.	233 Lbs.
Magnetic Tape Reader	156 Lbs.	196 Lbs.
MT/SR (Record Only)	226 Lbs.	266 Lbs.
"Selectric" I/O for MT/SR	70 Lbs.	74 Lbs.
Desk for MT/SR	225 Lbs.	225 Lbs.

#### ELECTRICAL REQUIREMENTS

Available for operation on 115 volts 60 cycle ONLY. Other voltages and/or frequencies available only by Special Engineering Request (S.E.R.).

#### CURRENT DRAIN

"Selectric" Composer	115V, 1.2 Amps
MT/SC or PT/SC (Includes Console, Reader(s) & Modified Composer	5.0 Amps
MT/SR (Includes "Selectric" Input Writer)*	2.5 Amps
MT/SC & PT/SC (Includes Console, Reader(s) & Modified Composer)	6.2 Amps
Model II or IV*	4.0 Amps

\*When determining current requirements for a system, figures for all recorders (Model V, II or IV) must be added to those for the MT/SC or Paper Tape "Selectric" Composer.

## OPERATION

Let's consider the mechanics required to manually do the various operations that are automatically done on the MT/SC.

The following sentence is to be justified to fit a specified line length or unit measure.

"The electronic logic used in the CCU is in the SLD family."

Before attempting to arrive at a solution for justifying the sentence, we must decide on a few variables. How much space do we want between words? How little space can we allow so that the words won't tend to run together? Let's say 3 units. How large a space can we tolerate without destroying readability? Let's say 9 units. We decide that a four (4) unit space would be ideal. We must also decide on the line length or measure in units. Let's use 150 units. This gives us a starting point for our solution.

At this point we look up the escapement value of the first character in the sentence. The escapement value of the "T" is 7 units. Does this exceed our line length? NO! Look up the escapement value for the "h". The unit value is 6 units. Add the 6 units of the "h" to the value 7 units of the "T" for a total of 13 units. Does this exceed our line measure? NO! Look up the escapement value of the "e". This is 5 units. Add 5 units to the 13 for a total of 18 units. Does this exceed our line measure? NO!

Next is the space. We have decided on 4 units so we select a four unit space and we must also remember that we have spaced and how many total spaces we have thus far. Add the four units of space to the total of 18, giving us a new total of 22 units thus far. Has this exceeded our line measure? NO!

We will continue the above routine - checking character escapement value, number of spaces and space value and always comparing the total escapement against the selected line measure of 150 units until we fill the line length to the next space. We calculate to the next space so that a word will not be broken - else we will have to hyphenate.

Now we must check our calculations to see how many spaces we have to work with to justify our first line.

Assume we have 5 spaces. Let's subtract 1 unit from each space. Are we within our desired line measure? Assume No! We are now down to a 3 unit space (we started with 4). We have previously decided that anything less than 3 units per space would be undesirable so let's backtrack and drop off the last word and again calculate. Assume our total line measure is now less than the desired line measure of 150 units.

We now have a line measure we can work with - but we must subtract one space (we backed up one word) from our total of 5, leaving us only 4 spaces to justify the line.

Now we will add 1 unit to the first of our 4 spaces. Does this fill our line measure? Assume No!

Add 1 unit to the next space (the first two spaces are now 5 units and the last two are 4 units).

If this does not exceed our line measure we will continue adding units to each space until all four spaces are 5 units. If this does not exceed our measure we will repeat the process, i.e., 6,5,5,5, 6,6,5,5, 6,6,6,5, etc. until the line measure and total units are equal or until we have reached the maximum of 9 units per space which we determined was the most we could use. If the maximum of 9 units per space was reached before the line measure is filled a decision must be made to either add the previously dropped word and hyphenate or to add inter-letter units to expand the line.

As you can see, many calculations must be made, and decisions must be made on the results of the calculations.

The calculations required to perform the functions illustrated are simple arithmetic computations using only addition, subtraction and comparisons.

In order for a machine to perform the same functions, the ability to perform these and other simple instructions is needed. A machine must be able to accept and retain characters. It needs to transfer the data from one area to another, and it must have the ability to output the finished data to a printing device. Also, the machine must have the ability to react to the results of its calculations.

Basically, three types of operations are required to arrive at the solutions for the different modes of operations used in the MT/SC. They are:

1. Input-Output Operations
2. Arithmetic Operations
  - Add
  - Subtract
  - Compare
  - Transfer
3. Jumps from one set of instructions to another set depending upon various conditions and results of computations.

The arrangement of the afore-mentioned basic steps is the secret of successful handling of typographical solutions. Each step is installed in the magnetic core storage of the MT/SC.

The MT/SC uses this core storage media in performing all calculations and operations as well as for storing the program steps. The core storage memory is truly the heart of the machine.

For the moment let's consider the memory to be a rectangle. Inside this rectangle are 16,384 ferrite cores, each of which can contain one bit of information.

An MT/ST tape has the ability to retain up to 8 bits of information per recording track. Likewise, the MT/SC deals with 8 bits of information as its smallest unit during an instruction time. Each 8 bit group in memory is called a BYTE. The largest group of cores dealt with in any one instruction time is 2 Bytes or 16 cores, called a REGISTER.

Each program step installed in the memory is one register in length. There are 32 registers in the lower part of memory numbered as Bytes 0 through 63. These so-called low order registers are used as working registers. In other words, the data changes frequently in this area of memory. Bytes 64 through 197 are used for table look-up (character escapement values). Bytes 198 through 315 are reserved for Output data. Bytes 316 through 465 are used for Input data.

Above this area, is the Program Step area of memory. As previously mentioned, each program step is one register (2 bytes) in length. All registers are numbered in even numbers. The area allocated for the program steps are bytes 466 through 2041.

There are 3 registers at the very top of memory used as work-

ing registers and are called SPECIAL WORDS. The purpose of the 3 special registers will be discussed in detail in the machine operation section. Figure 1 shows the memory allocations.

The magnetic tape or paper tape prepared for the MT/SC will contain composition material and may contain instruction codes as well. The tape is read by the proper reader and transferred to the CCU via the input interface. The data is transferred to one of the low order working registers and later to the input area of memory. This data is then operated upon according to the instruction codes on the tape and/or by instructions keyed in by the operator. After the data has been processed it may then be transferred to the Output area of memory and sent to the Translator and Composer for print-out of camera ready copy.

SPECIAL REGISTER	BYTES 2046 – 2047
SPECIAL REGISTER	BYTES 2044 – 2045
SPECIAL REGISTER	BYTES 2042 – 2043
<p>PROGRAM STEP AREA</p> <p>BYTES 466 – 2041</p>	
INPUT AREA	BYTE 316 – 465
OUTPUT AREA	BYTE 198 – 315
TABLE LOOK-UP	BYTE 64 – 197
WORKING REGISTER	BYTE 0 – 63

Figure 1



## MAGNETIC TAPE READER

### INTRODUCTION

The TAPE READER is basically an MT/ST tape deck that has been rewired to serve as a reading device. The reader can not record. The operator controls provide the operator with the ability to load and unload the right or left tapes, to search both tapes, to reread a track on the tape if an error occurs, and to skip the error if a reread operation does not clear an error condition. A cover unlock button releases the tape covers for removal of the unloaded tapes. The lower frame of the tape reader contains only the sense amplifiers and the magnet drivers for the magnets and solenoids in the tape deck. The sense amps were installed in the MT/SC console because of the noise (erroneous voltages) that would be picked up in the long wires between the reader and the MT/SC console.

### READ OPERATION

The purpose of a read cycle is to read one character from the magnetic tape, store the character in the Input Data Latches, to perform an odd bit parity check and to increment the tape if a valid character is read.

### LOGIC

A READ COMMAND (RC) signal is developed during an Input program step. The read command signal indirectly turns on a magnet driver and the reader cycle clutch is picked. The magnet driver circuit operates similar to the thyatron circuits in the MT/ST. When the input conditions are satisfied, a ground is supplied to one side of the magnet coil. The other side of the coil is connected to the +48 volt supply.

The emitter arm sweeps through the emitter coils and the head sweeps across the tape reading the bits serially just like the MT/ST. The method used to transfer the bits to the bit register is unique, however. An SLD counter is used to define which bit is being read. The counter is controlled by the MPS signals that are generated by the emitter arm as it sweeps through the emitter coils. The coils are divided into two groups. The odd numbered coils are series wired in one string and the even numbered coils are series wired in another string. The two signals generated by these strings are called MPS A and MPS B. These two signals are used to change the state of five latches which serve as a counter. If a bit is sensed while the counter is at count one, the one bit DATA LATCH is set. If a bit is sensed while the counter is at count two, a two bit Data Latch will be set, etc. The Data Register is composed of 9 latches, one for each bit position on the tape including the search bit position.

The Data Register serves as an interface between the MT Reader and the MT/SC console. Once the latches are set they will remain set until a reset signal turns them off. The reset signal

will become true after the bits are transferred to the processor's memory during an Input program step.

### PARITY CHECK

The outputs from the Data Register set up conditions in three parity circuits so that an odd bit parity check can be made on the first three bits, the second three bits, and the third three bits. The outputs of the three parity circuits, named X parity, Y parity and Z parity, are then anded together so that an odd or even condition can be determined for all bits read.

A device 1 CHARACTER READY signal comes true during 10 Count if an error has not occurred. If even parity occurs, character ready will not be true and the error light will come on.

If odd parity is satisfied during 10 Count the INCREMENT signal comes true. This signal turns on the stepping magnet driver and the tape steps because the 48 volts is supplied to the proper magnet through its respective pressure pad switch.

### MT COUNTER

The latch counter used to control the Data Register is composed of five latches whose outputs are named MT Counter A through MT Counter E. The first two signals, MT Ctr. A and MT Ctr. B, are controlled by MPS A and MPS B. Other states of the counter are controlled by the MT Ctr. A and MT Ctr. B signals. The states of the counter for determining any particular counter time are shown in the timing chart. Count 1 is identified by MT Ctr. A up, MT Ctr. B down, MT Ctr. C down, MT Ctr. D down and MT Ctr. E down. If a bit were sensed with the counter in this condition it would be set in the 1 bit latch. A bit sensed with the counter at Count 2 would be set in the 2 bit latch, etc.

The starting conditions of the counter comes from a signal called SET 0. The Set 0 signal resets all of the MT counter latches except MT Ctr. D. The cycle clutch is picked and the MT Reader begins its cycle. As soon as the emitter arm magnet couples the first emitter coil an MPS A signal is generated. Since MT Ctr. B was off, the Not MT Ctr. B level is up. Not MT Ctr. B is anded with MPS A, MT Ctr. A is set and Count 1 results. MT Ctr. D will be reset by the —MT Ctr. C, —MT Ctr. B, and MT Ctr. A leg of the reset circuit.

With MT Ctr. A up, the next emitter output, MPS B will set the MT Ctr. B latch. With MT Ctr. A up, MT Ctr. B up and all other latches down we are in Count 2.

The next MPS A, which is the output of the third emitter coil, resets MT Ctr. A. MT Ctr. B stays on. With MT Ctr. B set, MT Ctr. A off and all other counter latches off, MT Ctr. C sets. With MT Ctr. A down, MT Ctr. B up, MT Ctr. C up and MT Ctr. D and MT Ctr. E down we are in Count 3.

All other conditions of the counter through 10 Count can be determined by the latch counter timing chart. Other And/Or legs of the counters are used to set up 13 Count, 14 Count and 15 Count to identify Unload, Search and Load operations.

## LOAD

The purpose of the load left or load right keybutton is to advance the tape from the cartridge to the pre-recorded portion of the tape. Pressing the load left or load right keybutton will result in loading the corresponding tape. The tape is advanced forward at high speed until the rewind slot is detected by the rewind sense switch. Then the tape is read until a feed code is detected. Tapes prepared for the MT/SC must have a feed code recorded on the tape prior to any recorded text or control codes. After the feed code is read the MT Reader cycle clutch latches. The feed code is stored in the reader interface (Input data latches) and the reader steps to the next recorded track and stops.

## LOGIC

Although the load function of the MT/SC is similar to the load function of the MT/ST, different logic is used.

In order to get a load operation the tape must be in an unloaded condition. A ground will be supplied to the load buttons through normally closed Leader Sense Left B or Leader Sense Right B contacts. The ground levels go to load left or load right keybutton switches. When either of the switches are depressed, a ground is supplied to their respective integrator circuits. The integrator circuit merely eliminates contact bounce caused by the wiping of the dry contacts of the load switches. The ground level supplied by the load switch results in an up level at the output. The load left or load right signal is fed into a circuit whose output is named SET 15 and into a station address latch. If the load right button had been depressed, the station right portion of the latch would set. Load left would select station left by resetting the station address latch. The Set 15 signal goes to an up level and will set the reader counter to Count 15.

The method of setting the counter is as follows:

MT Ctr. A	If MT Ctr. A were latched at an up level it would be reset when Set 15 goes up. If MT Ctr. A were down already nothing would result.
MT Ctr. B	MT Ctr. B must be set to get a Set 15 in the counter. If MT Ctr. B were down, Set 15 would set it.
MT Ctr. C	MT Ctr. C is reset in the same manner as MT Ctr. A.
MT Ctr. E	MT Ctr. E is reset in the same manner as MT Ctr. A.
MT Ctr. D	MT Ctr. D is set in the same manner as MT Ctr. B.

With the Counter in Count 15 a signal named 15 COUNT becomes true. When 15 Count goes up the load search solenoid magnet driver is activated. When the load search contacts make the right detent solenoid magnet driver or left detent solenoid magnet driver will be activated. The magnet drivers are selected by LOAD-SEARCH SOLENOID signal (integrated signal from load-search solenoid contacts), station address latch and Not REWIND which goes down when the rewind slot is sensed. The tape moves forward at high speed because the detent is pulled and the load search solenoid is active. When the tape is loaded to the rewind slot and the rewind switch transfers, the integrated REWIND SENSE signal comes true. —RWD goes down and the detent magnet driver is turned off.

Rewind and Count 15 are Anded together and a READ latch is set. Read brings up a ST 0 level and the MT Counter goes to Count 0. Count 0 drops out the load search solenoid because the magnet driver inputs are no longer satisfied. The pressure pad for the station addressed is up after the leader sense switch transferred for the station addressed. Set 0 also resets the Data Register. The cycle clutch is picked at Count 0 when the pressure pad is up and we are not re-reading. One cycle results.

The MPS A and MPS B pulses step the counter and parity is either satisfied or dissatisfied. Obviously nothing will be read until the oxide portion of the tape comes under the head. The Read latch will stay set and other cycles will occur. The Reader will read and step until a feed code is set in the Data Latches.

When the feed code is set in the data latches, CR RET comes true. When CR Ret goes up the Read latch is reset and the Reader cycle clutch latches. The feed code is latched in the Data Latches.

If a second tape is loaded, it will follow the same load sequence as the first.

## UNLOAD OPERATION

The purpose of unload is to return all the tape into the tape cartridge so that the cartridge may be removed. Tape may be unloaded from either station by depressing the unload button associated with that station. The unload buttons will latch down when depressed and remain down until the load button for that station is depressed.

A single cover unlock button will energize the cover unlock magnet for either station provided the tape is unloaded completely.

## LOGIC

The unload logic is basically all contact logic. When we depress one of the unload buttons, the Unload Contact in series (and circuit) with the Leader Sense N/O contact will pick the Hi Bias Solenoid, the Detent Solenoid and bring up a signal called END OF TAPE OR UNLOAD (EOT+UNLD). This signal is used to bring up COMMON RESET which sets the counter to 13 Count to define the unload operation and to turn on the EOT light.

With the Detent Solenoid picked and Hi Bias picked the tape returns into the cartridge at high speed reverse. As soon as the Leader Sense N/O contact opens, the voltage path to the Detent and Hi Bias Solenoids is opened.

A diode across these coils delays their drop to insure the tape will be fully seated in the cartridge. The Leader Sense N/O also drops EOT+UNLD which drops Common Reset and the EOT light.

The tape is now unloaded. The unload button is still latched down, the counter is at 13 Count and the Leader Sense N/C now provides a path to the cover unlock solenoid and cover unlock key so that the tape may be removed.

### SEARCH OPERATION (RIGHT)

The purpose of a search operation is to advance the tape at high speed until the next reference code is located. After the search bits are detected, the high speed operation is terminated and the Reader cycles reading the tape until a carrier return code is stored in the Data Latches.

On the MT Reader a depression of the search key always causes the right station to search first. At the end of this operation the reader will automatically initiate a search operation on the left tape, providing the left station contains a tape and it has either been previously loaded or searched.

The MT Reader does not contain a reference selector dial; therefore, the depression of the search key causes the tape to be searched forward to the next reference code. In order to locate a reference code that has previously been searched to, the tape must be unloaded and researched.

### LOGIC (RIGHT)

When the operator depresses the search key, the Search Key Contact is anded with Leader Sense Right B N/O to provide an integrated signal called SEARCH KEY. This signal in turn brings up a signal called Set 14 which conditions the five counter latches for 14 Count. With 14 Count true, Search and Station Right come true. If the left station contains a tape that is loaded, 14 Count will also cause TRANSFER to come true. This Transfer signal will be used later to cause a search operation on the left station after the right station search operation is completed.

Search causes the Load Search Solenoid to be energized, the Search Position Magnet to be de-energized, and picks the Cycle Clutch. The Reader takes one cycle and the head latches over the search channel, closing the search position contact. The counter is inhibited from counting due to —Search being down. An integrated signal SEARCH POSITION comes true when the search position contact closes. This signal is anded with LSSS (an integrated Load Sch Sol Contact signal) and the Detent Right Solenoid is picked. When the Detent contact makes an integrated signal called DETENT OUT comes true.

Now that we have the Load Search Solenoid and the Detent Right Solenoid picked the tape is moving high speed forward with the head latched over the search track.

When the search bits are sensed by the head and sense amp, a signal called SEARCH BIT is developed. Search Bit is anded with Detent and Search Position and Read comes true. Read drops the detent solenoid to stop the tape and picks the Search Position Magnet to allow the head to return home. With the Home Contact made and Read true, Set 0 comes true. The counter sets to 0 Count, the Data Latches are reset, the Load Search Solenoid drops, Search goes untrue and the Cycle Clutch is picked.

With the cycle clutch picked the machine cycles reading the tape until a carrier return code is decoded. The Read signal goes down, the cycle clutch latches at the end of the cycle and the carrier return code is latched in the Data Latches. This completes the search operation on the right station.

### LOGIC (LEFT)

Upon the completion of the search operation on the right station the head is at home, the counter is at 10 Count, Read is untrue and Transfer which was set during search right is still true.

With these conditions STATION LEFT comes true and Search comes true again. Search resets Data Latch 3 (carrier return code from search right operation).

Logic from this point is identical to search right with the exceptions that Detent, Station and Contact logic pertain to the left station, and the fact that when Read comes true after the search bits are detected, it will not only drop Detent Left Solenoid and bring up Search Position Magnet, but will also drop the Transfer signal.

The head goes home, Set 0 comes true, the Cycle Clutch is picked, and the machine cycles until the carrier return code is decoded. The carrier return code is latched in the Data Latches and the machine stops with the left pressure pad still up waiting for instructions from the Composer Control Unit (CCU).

### REREAD

When a playback error occurs on either station, the error light comes on. The Increment Latch fails to set, and the tape does not step. The purpose of Reread is to recycle the Reader and reread the same character. Also any information stored in the Data latches from the error cycle must be cleared.

### LOGIC

Depressing the Reread key opens a normally closed contact which brings up the signal REREAD. With the head at home, Reread and Home will cause Set 0 to come true. Set 0 will clear the Data Latches and set the counter to 0 Count. All conditions for picking the cycle clutch are now true except —Reread.

As soon as the Reread key is released, Reread goes down and —Reread comes true. The Cycle Clutch is picked and a read cycle occurs.

## SKIP

If a playback error is detected and reread still causes a playback error, then the invalid character on the tape must be skipped to allow the tape reading to continue. The purpose of the Skip Key is to cycle the reader and increment the tape past the invalid character.

## LOGIC

Depressing the skip key brings up two signals, SKIP and REREAD. The Skip signal will cause SET LOW to come true, setting the LOW LATCH. This will allow a change in the program routine to cause the printer to space 9 units and allow room on the hard copy for manual correction of the lost character.

With Reread true and the head at home, Set 0 comes true to reset the counter to 0 Count and clear the Data Latches. All conditions for picking the cycle clutch are now true except —Reread.

When the Skip key is released, Reread goes down and —Reread comes true. The cycle clutch is picked. Set Low is still true since it is a latch and has not been reset. The Set Low signal causes ODD to come true and stay true even though invalid information is read from the tape. Therefore, at 10 Count the Increment signal comes true to step the tape past the invalid character without error.

## DATA FLOW

Most operations done by the MT Composer require processing data that has been inputted into or contained in the core storage memory. Four cores from each of two memory locations can be read and operated upon during each CCU cycle. The normal cycle is composed of two READ operations followed by two WRITE operations. Each cycle is called a BIT TIME. Four cores, or bits of data, can be read during each Read portion of the bit time cycle. The first read cycle is called P-READ TIME and the second is called Q-READ TIME. During P-Read Time four cores are simultaneously read from a defined location in memory. The bits read from these four cores are

sensed and amplified by four sense amplifiers. These amplifiers set four triggers which are part of the sense amplifiers' circuitry and are called the Q-TIME BUFFER. When the triggers set, the data is also set into a four latch register called the P-TIME BUFFER (Fig. 1). After latching the first four bits into the P-Time Buffer the Q-Buffer is reset. A second location in memory is selected for Q-Read Time. At Q-Read Time, the first four cores of the second memory location is read and sensed by the sense amplifiers. The amplifiers again set the four triggers in the sense amplifier circuitry. With the four bits of data from the first memory location latched in the P-Time Buffer and the four bits of data from the second memory location set in the Q-Buffer, the two pieces of data are merged in an And type accumulator.

Two WRITE CONTROLS, used to control current sources into memory, are available for writing data back into memory. One control is the Write P-Buffer control and it is used to write unaccumulated data into memory. The second control, Write from the Accumulator, is used to write merged (accumulated) data into memory. The write portion of the bit time cycle is a Q-Write operation followed by a P-Write operation. The data to be written during the Q-Write portion of the bit time cycle will be written into the same four cores from which the Q-Read data was acquired. Likewise, the P-Write data is written into the same four cores that were read during the P-Read cycle.

During the complete cycle, P-Read, Q-Read, Q-Write and P-Write four cores from each of two memory locations were operated upon. In order to perform read and write operations on complete registers, four bit time operations are done. Each bit time is different only in respect to the cores being read and written. After each bit time, the memory selection circuitry merely steps to the next four cores until 16 cores from two memory locations have been operated upon. A CARRY OVER LATCH is used in cases where the accumulated data results in a carry digit between bit times. The four bit times used to operate upon registers is called one INSTRUCTION TIME. Several Instruction Times are required to perform each program step. However, the data flow path is similar in each case.

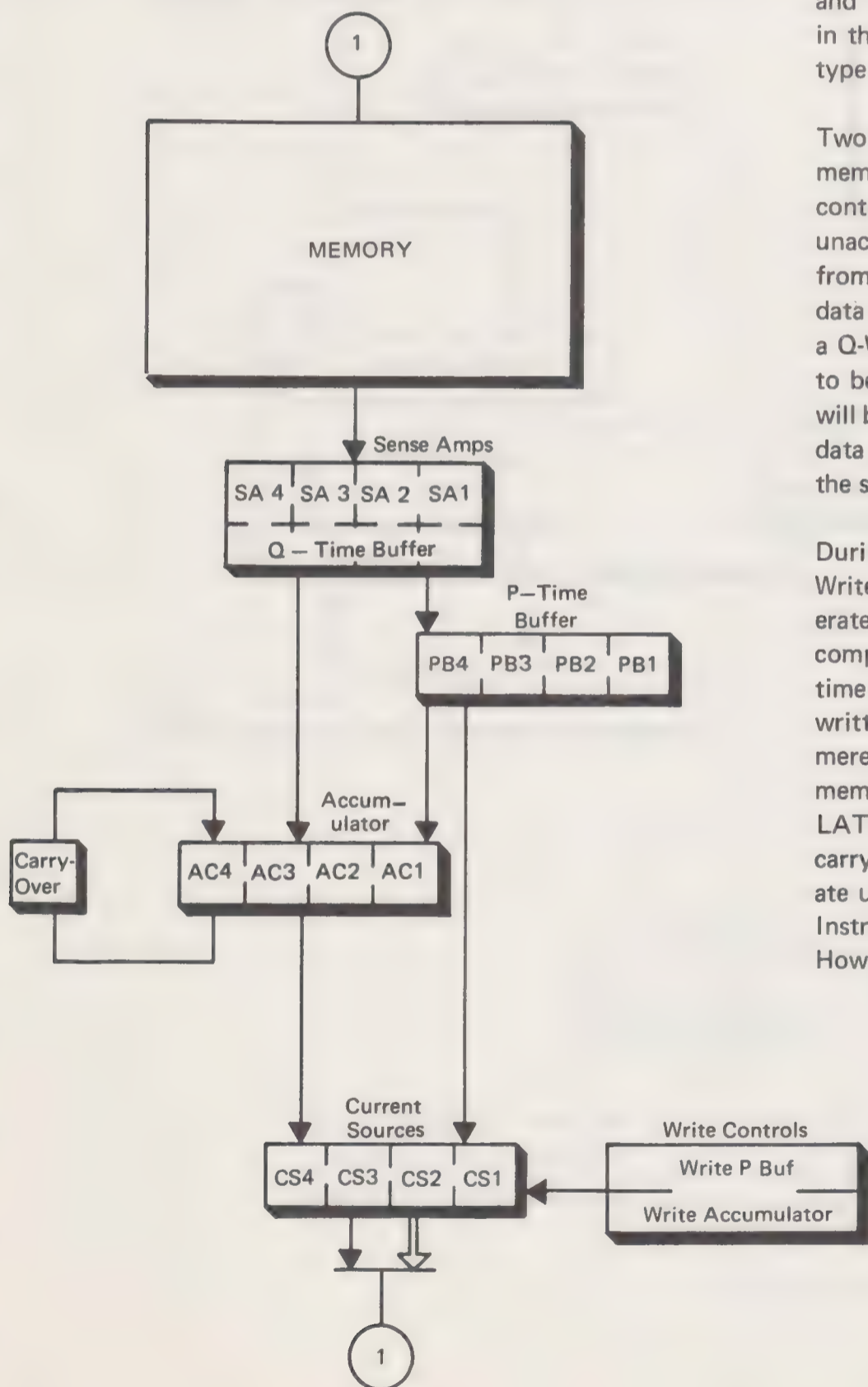


Figure 1

the reader Data Latches is written into memory. Input from the Console Keyboard follows the same data path except no Data Latches are required for keyboard input.

Output requires that information from memory be sent to an output device. Data for output is read from memory, sensed by the sense amps, and latched in the P-Time Buffer. The data is transferred to an OUTPUT REGISTER four bits at a time until the completion of the fourth bit time. The data is then outputted either to the Translator or to the Lights depending upon the conditions set by the I/O control.



## MACHINE ORGANIZATION

The organization of the Composer Control Unit evolves around the CORE STORAGE MEMORY. The Memory contains the Program, Input/Output allocations, Working Registers and Special Areas. It is apparent that control must be maintained in order to get the correct data into and out of memory. Our paths of data flow require that we gather data from two different locations in memory during each bit time cycle. To address the proper location in memory at the proper time, it is necessary to control our memory addresses relative to time. A 17 latch free running CLOCK is used in conjunction with 11 MEMORY ADDRESS LATCHES to control the addresses (Fig. 3). The Memory Address Latches alone have the ability to address only one location in memory during each Instruction Time (4 bit times). In order to address a second memory location, Clock signals are used to control the address. Signal levels developed by the Memory Address Latches are combined with signals developed by the Clock in circuitry named the MEMORY ADDRESS DECODE. Clock signals alone can cause the MA decode to address the portion of memory allocated to special words. All portions of memory other than the special words require decoding the Memory Address Latches in conjunction with Clock signals to choose the proper line to memory.

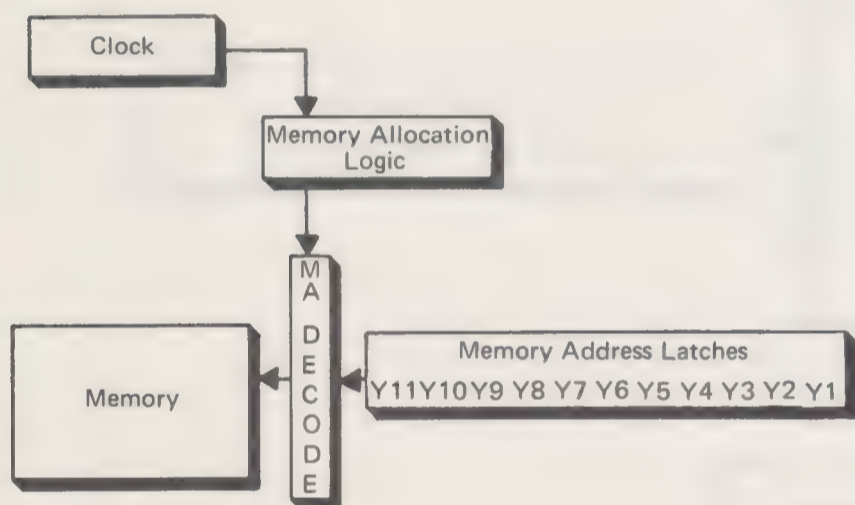


Figure 3

One register in the special area of memory is used to store the address of the next program step to be done by the CCU. When the power on switch is activated, program step address 546 is written into this special register in memory. This PROGRAM STEP ADDRESS REGISTER will be addressed and read under Control of the Clock (Fig. 4). The 546 will be read and sensed by the sense amps, four bits at a time, during the P-Read portion of four bit times. The data from this Program Step Address Register will be set in the P-Time Buffer as explained in Data Flow. While the program step address is in the P-Time Buffer the Memory Address Latches are set. This is essentially a transfer operation. If 546 was read from memory the respective Y latches would be set to address register 546. During this same cycle the quantity 2 would be added to the 546 read from the Program Step Address Register in memory. The accumulated amount, 548, would be written into the Program Step Address Register so the location of the next step to be done is available.

The Memory Address Latches can be set several times while performing program steps; however, they can be set only once during any Instruction Time. In order to obtain data from two

memory locations during each Instruction Time, one address must be controlled by the Clock while the other address is primarily controlled by the Memory Address Latches. The Clock alone can address only Special Registers. The special registers are named the Program Step Address, the A-Word and the B-Word.

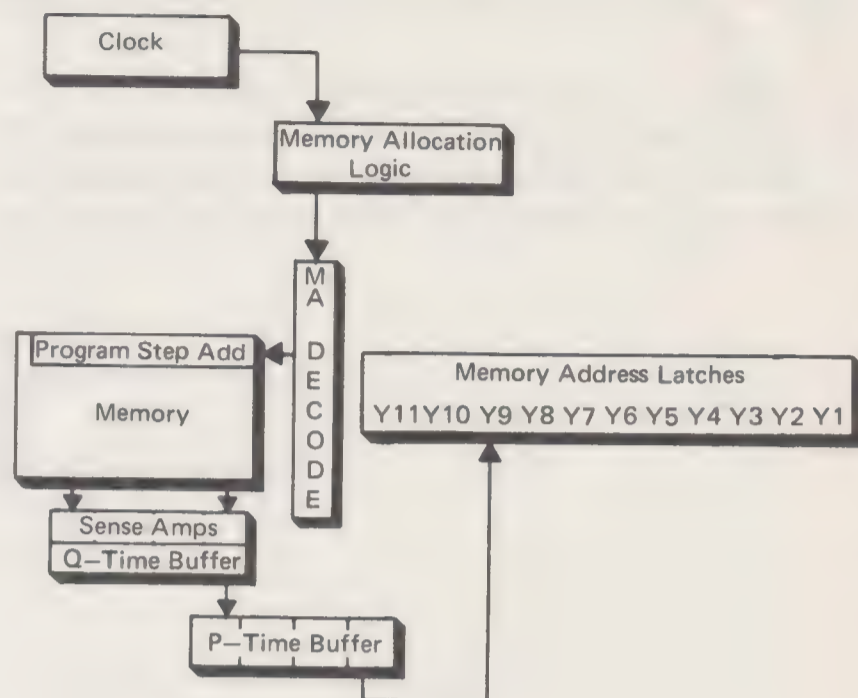


Figure 4

Each program step in memory contains several bits of data to identify the type operation to be performed. The coding (arrangement) of these bits is called the Operational Code. The program step must first be read from memory in order to determine what the CCU is to do. During the first Instruction Time (4 bit time cycles) we determined where the program step to be done is located. The address of the program step was set in the Memory Address Latches. We now use the address set in the Y latches (decoded through the MAL decode) to locate the program step to be done. The program step is read from memory during P-Read Time and the data from the step is set into the P-Buffer. While the data is in the P-Buffer, 7 latches, called OPERATIONAL CODE LATCHES, are set (Fig. 5). This is again a transfer operation. The Operational Code was transferred from the program step contained in memory to the Operational Code Latches.

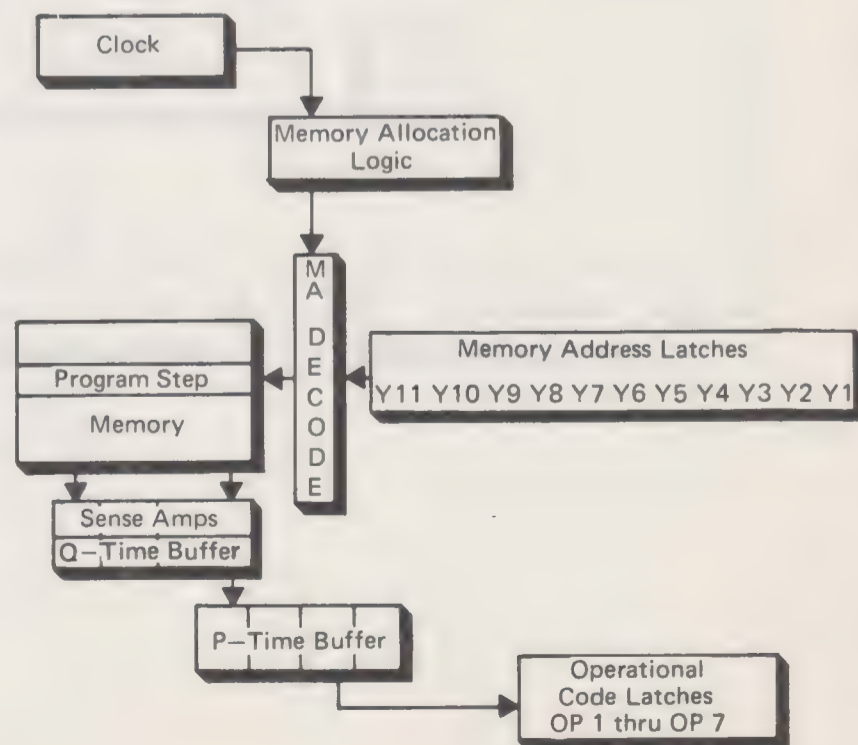


Figure 5

The Operational Code Latches are set only once during each program step. The latches remain set throughout the program step.

Some program steps done by the Composer Control Unit are simple and require only few Instruction Time Cycles while others are complex and require as many as ten Instruction Time cycles.

The Operational Code Latches provide control to the Clock and to the Memory Address logic so that the correct data will be operated on at the proper time. All program steps are accomplished by operating on the proper data at the proper time.

Some Instruction Time cycles require that data be transferred from one location in memory to another. Other Instruction Time cycles require that data be operated upon arithmetically. WRITE CONTROLS give the CCU the ability to write either unchanged data or accumulated data back into memory. The Write Controls are under control of the Clock. Since the Operational Code Latches regulate the Clock, the Clock can in turn operate the Write Control (Fig. 6). The Write Control signals are added with the outputs of the Accumulator and P-Time Buffer to control the CURRENT SOURCES into memory. The Current Sources control the actual writing of data.

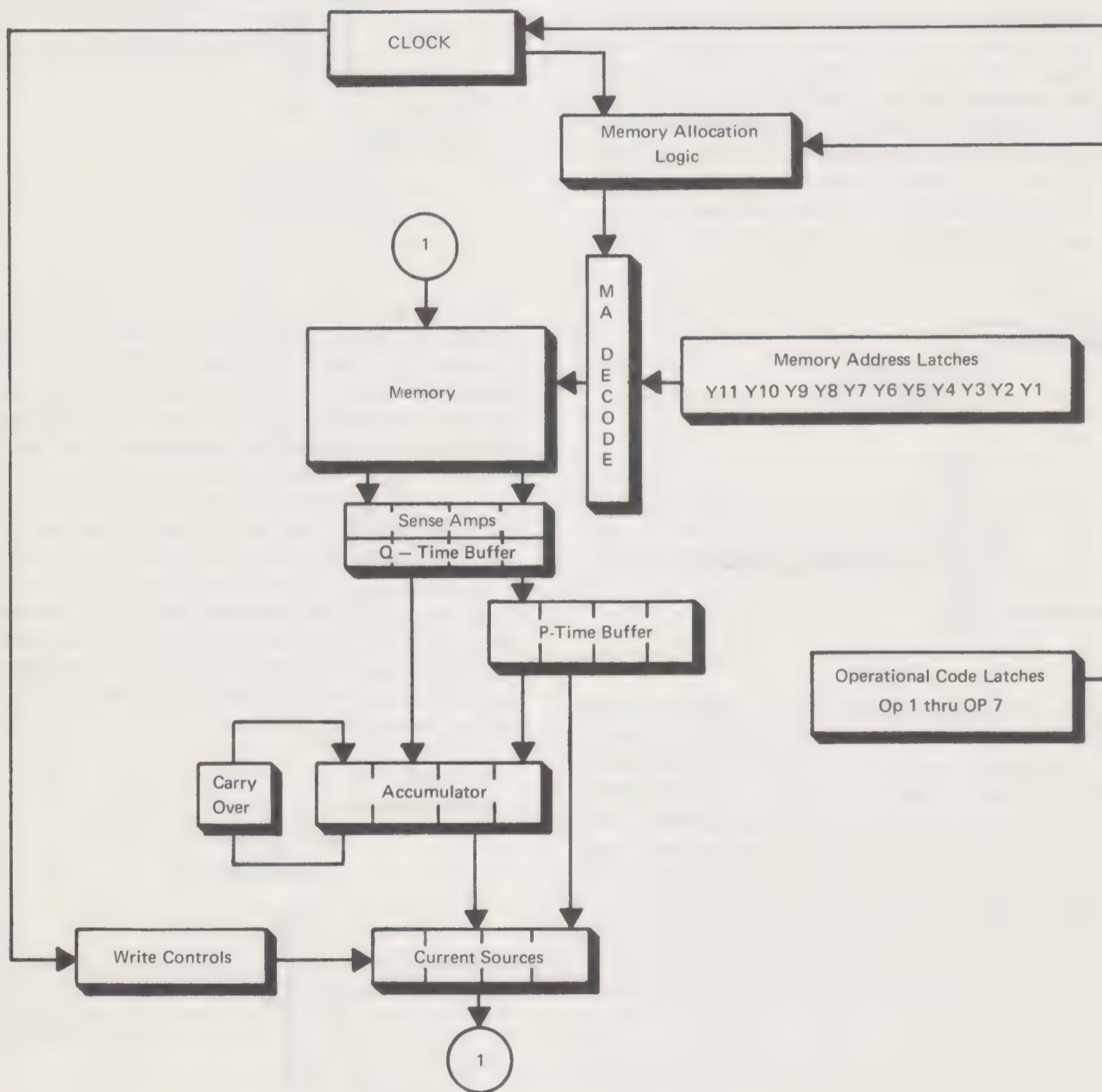


Figure 6

The LOW AND EQUAL LATCHES are used to determine if a conditional jump (decision) is to be done. The jump decision is dependent upon the results of various calculations. The Low and Equal latches are set by the Accumulator outputs or Input Devices. Since the results of all calculations are realized at output of the Accumulator, a hi, lo, or equal condition will be available (Fig. 7). If the Low and Equal latches match the conditions defined by the program step, operations must be done to address the program step that is defined in the jump step. If the Low and Equal latches do not match the conditions of the jump step, the step must be ignored. The Low and Equal latches regulate the Clock in conjunction with the Operational Code and its free running capabilities.

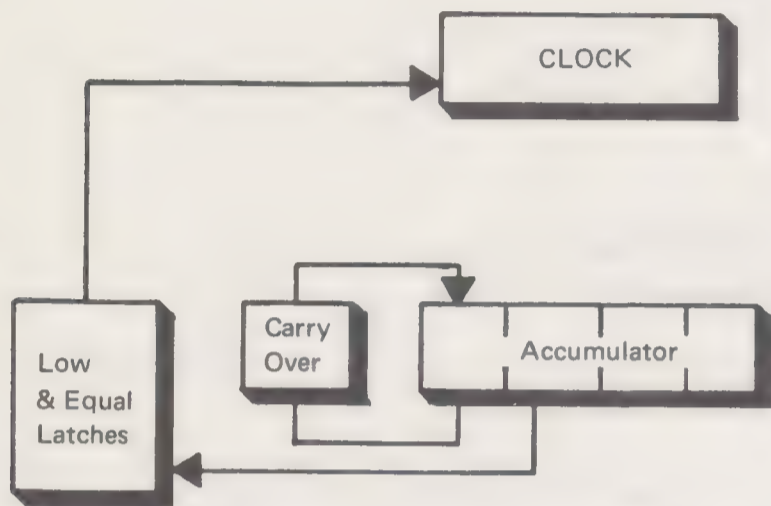


Figure 7

Thus far we have dealt with the machine organization necessary to internally operate the CCU. Input/Output operations require I/O Control logic. I/O Control merely identifies where data is to be received from or sent to. If an INPUT step is called for by the program step, the I/O control logic will direct the input from the Data Latches or from the Console Keyboard to the P-Time Buffer at the proper time (Fig. 8). If an OUTPUT step is called for by the CCU an 8 latch OUTPUT REGISTER will be set and the output data will be directed to either the Translator or Keyboard Lights. The Output Latches are set and will remain set until another output step arrives. Although the Output Latches are set for long periods of time, circuitry in the I/O controls prevent more than one mechanical cycle of the Translator for each time the latches are set.

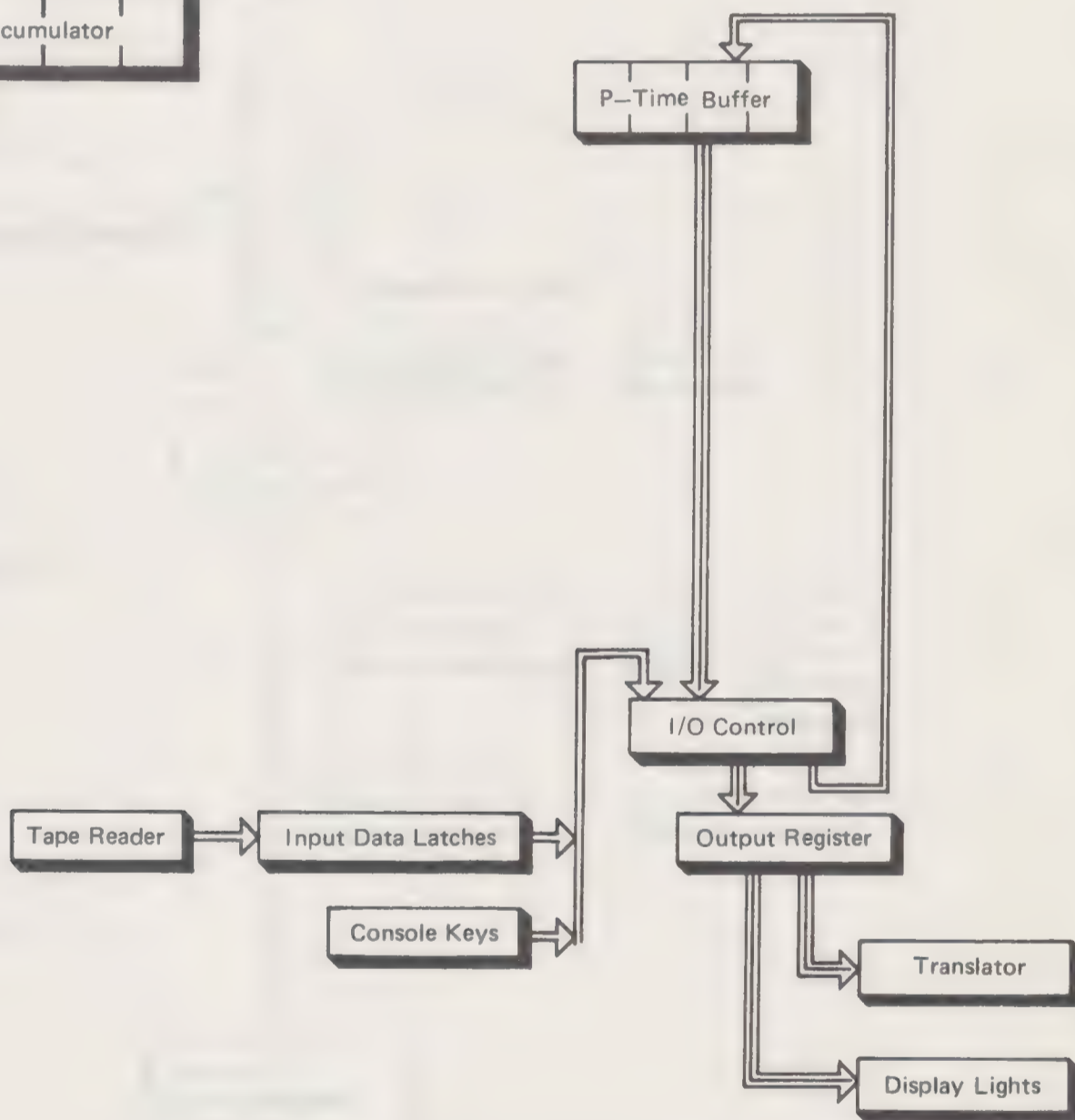


Figure 8

The following is a brief review of the components used to control data flow (Fig. 9).

1. **MEMORY** - contains the CCU program, working register, table look-up data, Input/Output data and special registers.
  - a. Memory Addresses - Clock signals and/or the Memory Address Latches select the locations in memory that contain the data to be operated upon.
  - b. Clock signals alone select the Program Step Address Register, the A-Word register, and the B-Word register (special words in memory).

- c. Clock signals combined with logic generated by the Memory Address Latches have the ability to operate upon any other location of memory. The Memory Address latches are set as data passes through the P-Time Buffer.

2. **OPERATION CODE LATCHES** - 7 operational code latches define the program step being performed. The latches control the Instruction Time cycles (clock) needed for any particular program step. The latches are set as data passes through the P-Time Buffer.

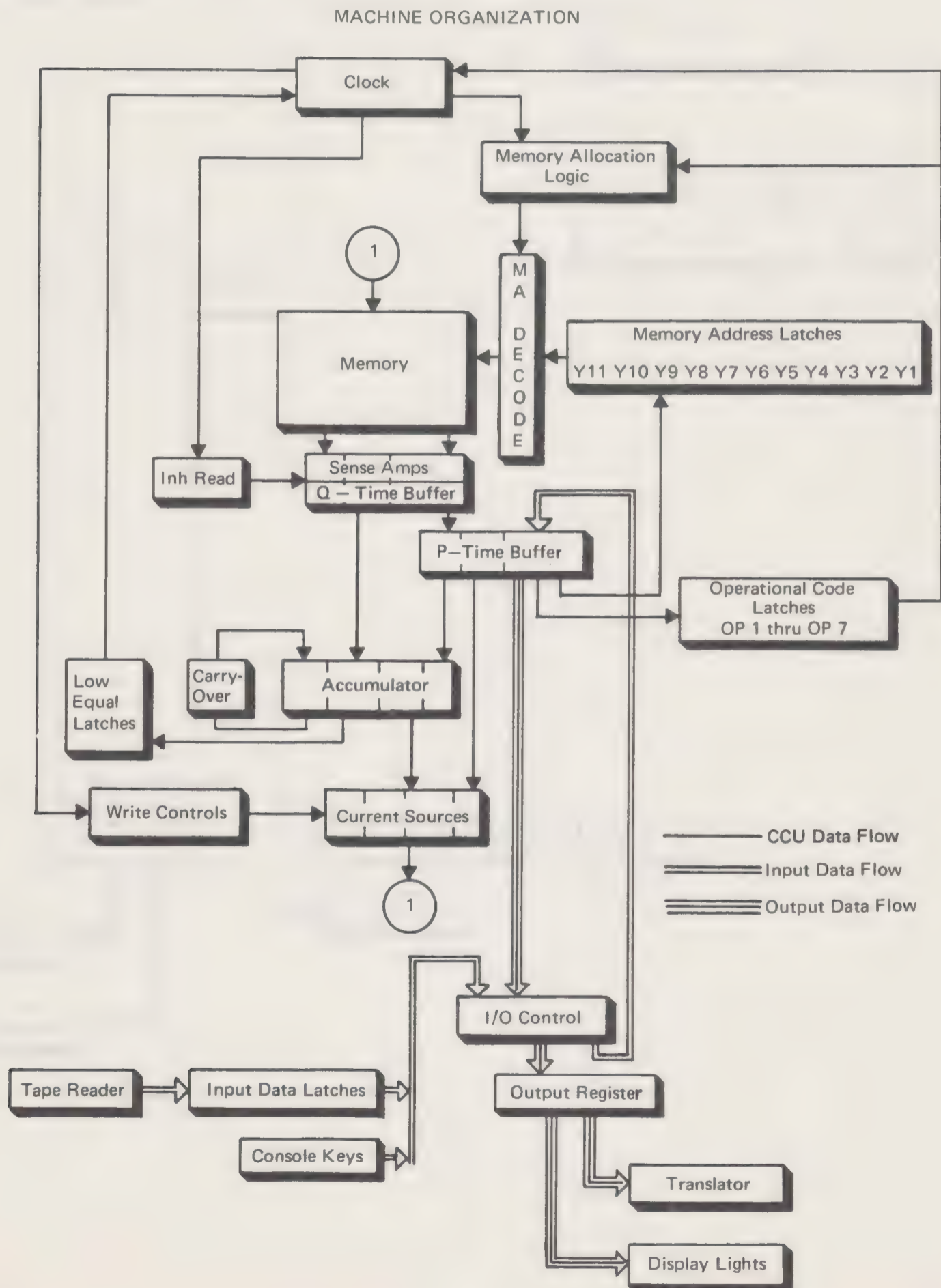


Figure 9

3. **CLOCK** - controls the times various locations in memory are addressed and controls the writing of data into memory. The Clock operates in a controlled free running state. The Clock is controlled by the Operational Code Latches and Low and Equal latches.
4. **SENSE AMPLIFIERS** - used to sense the bits of data read from memory. Four Sense Amps are used to read 4 bits at a time from memory. Data read from memory is set into the Q-Buffer and will remain there until reset.
5. **P-TIME BUFFER** - accepts data from the Q-Buffer during P-Read Time. Data can also be latched into the P-Time Buffer from the input interface.
6. **ACCUMULATOR** - merges data from the P-Time Buffer and data set in the Q-Buffer at Q-Time. The data in the Q-Buffer can be subtracted from or added to the data in the P-Time Buffer depending upon the program step being performed.
7. **CARRY-OVER LATCH** - is used when the results of a computation require the carry of a digit from one bit time to the next.
8. **LOW AND EQUAL LATCHES** - used to give an indication of the type result attained in any particular computation. The conditions of the latches are compared to conditions in various jump program steps to determine if jumps to other program sequences is required. The Low and Equal latch outputs control the clock during conditional jump program steps.
9. **CURRENT SOURCES** - used to control the writing of data into memory. The Current Sources are controlled by the Write Controls in conjunction with data in either the Accumulator or P-Time Buffer.
10. **WRITE CONTROLS** - two write controls, Write from Accumulator, and Write from P-Time Buffer are used to control the Current Sources into memory.
11. **I/O CONTROL** - controls data flow to and from input/output devices and the CCU.
12. **INPUT DATA LATCHES** - retain each character read by the tape reader until it is needed.
13. **OUTPUT REGISTER** - an 8 latch register used to retain data from the CCU until it can be operated upon by the selected output device.



### PROGRAM STEP SET

The program used to operate the Composer Control Unit (CCU) is installed in sequential registers. When the machine is turned on the first step addressed will be step 546. After step 546 is complete, we will perform step 548, then 550, and so on. At the completion of each step the results attained set, preserve or reset two latches. The latches are called the LOW and EQUAL latches. Since most steps performed by the Composer Control Unit are arithmetic, a sum, difference, or zero condition will be available. If the result is positive, the Not Low portion of the Low latch will be true (Example:  $4-2 = 2$  or  $2+2 = 4$ , positive or Hi). If a negative result were attained, Low latch would be on (Example:  $2-4 = -2$ , Negative or Lo). If the result of the computation were zero the equal latch would be set (Example:  $4-4 = 0$ , Equal latch set). These two latches give the machine the ability to make decisions. Normally, the program is done in sequential order. Let's say that step 650 is an arithmetic instruction. At the end of step 650, the results of the computation would set the Low or Equal latches. By using a **CONDITIONAL JUMP** step, such as jump to step 920 if Not Low is true, we would have the ability to change the program sequence on a condition. The jump step described would be step 652. If the Low latch were on, the program sequence would not change and the next step done would be step 654. The conditional jump step gives the CCU the ability to make decisions.

To fully explain the Program Step Set, let's use the example previously mentioned in the introduction of CCU operation.

"The electronic logic used in the CCU is in the SLD family."

Figure 1

- Let's assume the first step in the justify program is step 748 (see Fig. 2). Before accepting a character from the tape, we must first set up a condition that will tell us where to put the character. We always want the first character read to appear in the first Byte of the input block in memory (byte 316). We must install this quantity (316) somewhere in memory and use it as an address. Two steps will be required to set the address. Both steps will be Immediate Arithmetic operations. The Immediate Arithmetic step appears in memory as shown in Fig. 3.

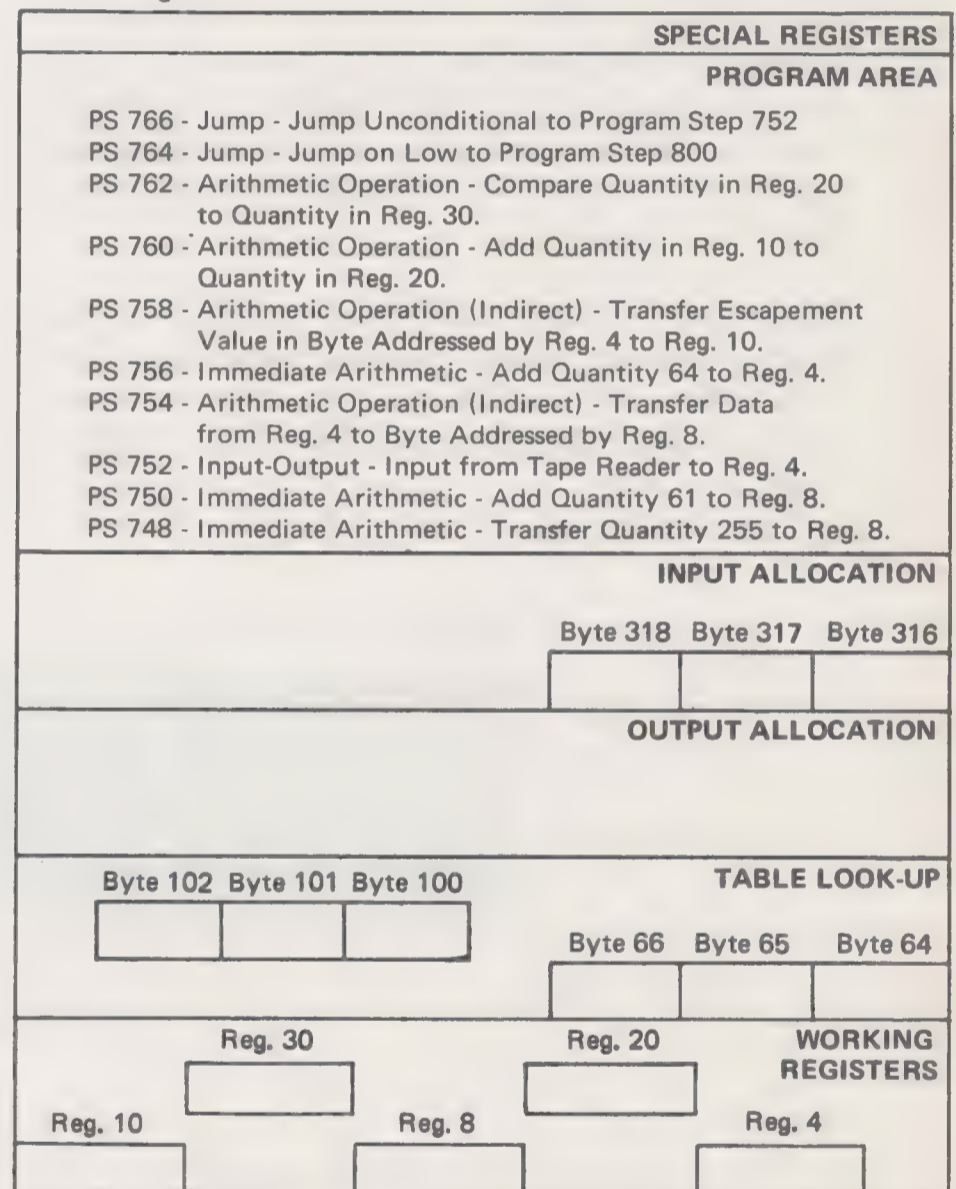


Figure 2

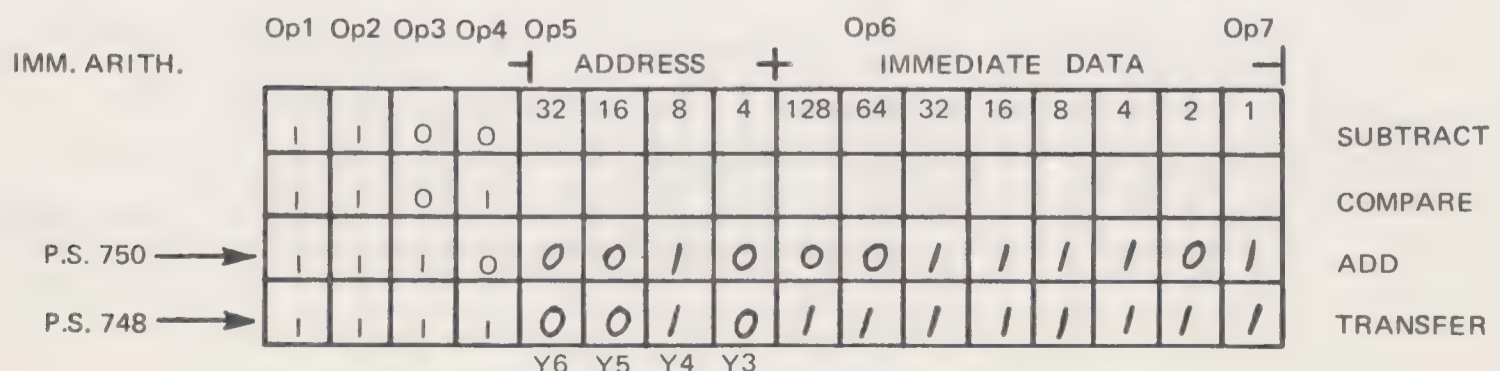


Figure 3

As you can see from the step, the largest quantity of data that can be contained in the program step is 255. All ones in the 8 bit positions allowed for data =255. In the first Immediate Arithmetic operation, we will transfer 255 to Reg. 8. The 255 in the program step will remain in the step.

Program Step 750 is an Immediate Add. The quantity 61 is to be added to the quantity already in Reg. 8. At the completion of P.S. 752, the quantity 316 will be in Register 8 (255 + 61 = 316). As previously mentioned, 316 is the address of the first byte in the input allocation memory.

The Immediate Arithmetic program step gives the CCU the ability to subtract, add, transfer and compare fixed data (up to quantity 255) to/from the data in Registers 4, 8, 16, 32, etc. up through Register 60 (divisible by 4).

- The next program step that must be performed is to input a character from the Tape Reader to one of the 32 low order working registers (Reg. 4). The input program step located at register 752 will appear in memory as illustrated in Figure 4.

Shaded areas are used to define the type Input-Output desired. The register area will contain the address of the register where the input data should go. Only the 32 low order working registers can accept data from an input device.

At the completion of the input instruction the bit configuration of the "T" (first character on tape) will be in Register 4.

All Input-Output program steps are similar except for the operational code, located in the shaded area. Input instructions are possible from the left or right MT stations, the Paper Tape Reader and from the console keyboard. The operational code in the input step defines from which unit the processor will accept information. The operational code also defines whether the lights on the keyboard or the translator will receive output data.

- The next step is to transfer the character "T" into Byte 316 in the input area of memory. For this step we will use an Arithmetic program step which will operate on data or addresses of data in two different low order registers. In this step we will do what is called a P INDIRECT TRANSFER. The indirect term means that we are using the register being operated on as an ADDRESS rather than for DATA. Program step 754 will appear in memory as illustrated in Figure 5.

In this case, we have the program step; transfer the data in Register 4 to the byte addressed by Register 8. At the completion of this step the "T" would be in Byte 316 and also in Register 4. In a transfer step we clear out the old data before transferring the new.

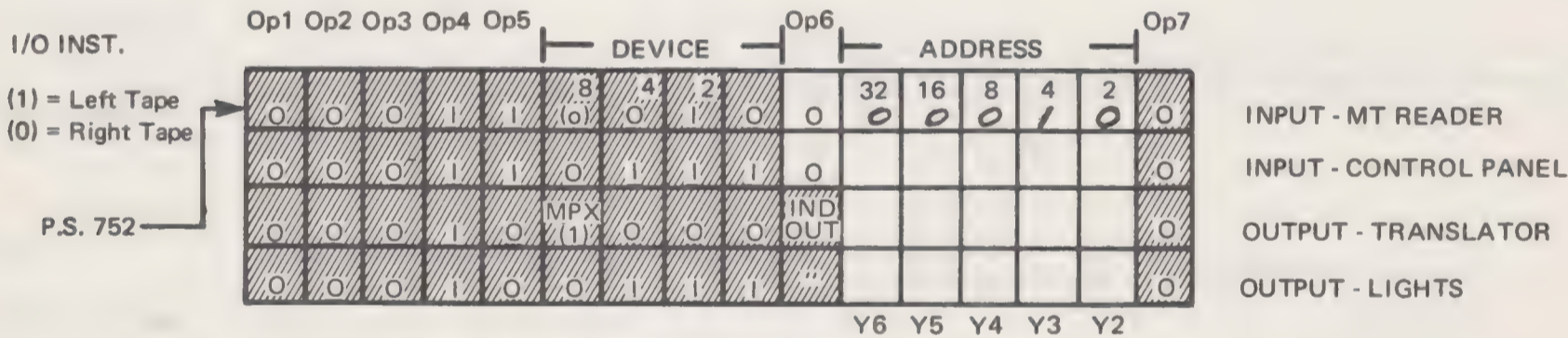


Figure 4

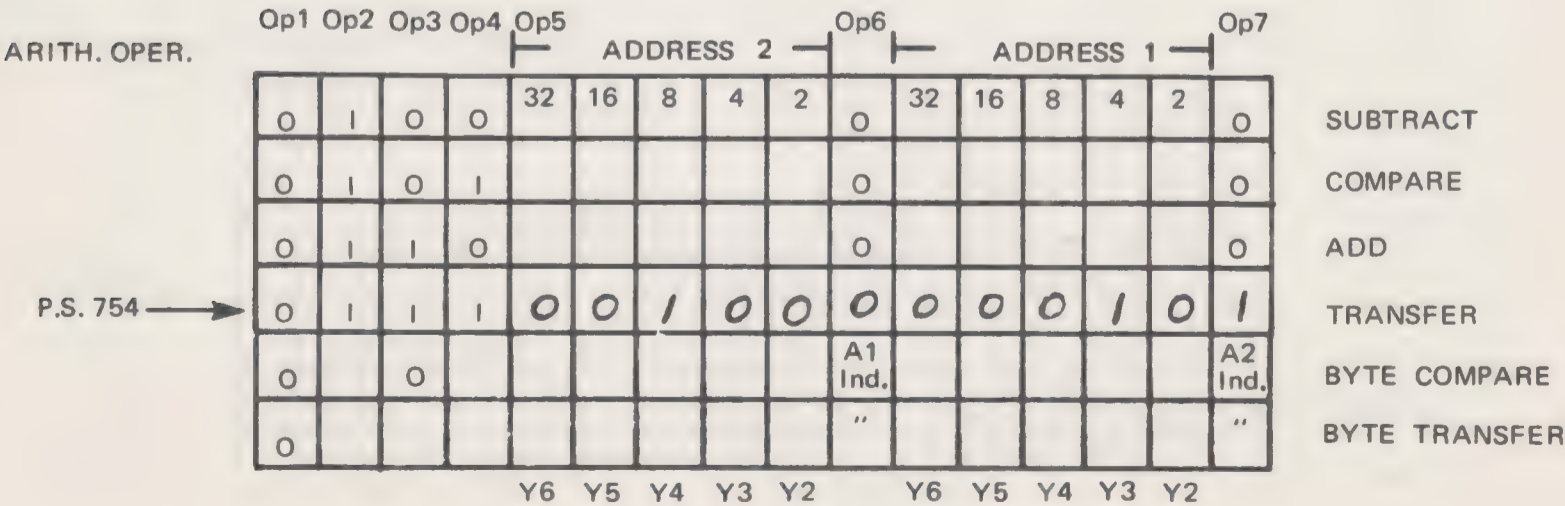


Figure 5

In an Arithmetic program step we can subtract, compare, add, or transfer the data in two different low order registers. We can also transfer or compare the data in either one of the registers to the byte addressed by the other register with a P or Q indirect operation. Either or both of the registers called out in the program step can be INDIRECT. If both are indirect the byte addressed by the Q register will be transferred or compared to the byte addressed by the P register. There is one other function that can be done during an indirect operation. The quantity "1" can be added to the address of the indirect register. This function is called a BUMP BY ONE. If both registers are indirect a "1" will be added to both indirect addresses. This gives us the ability to use the same program step over and over for transferring data to successive bytes. In other words, using our present example, we always input from the tape reader to Register 4. The first 3 characters on the tape are "T", "h", and "e". The "T" is transferred to Byte 316 because of the address that we installed in Register 8. If we bump the address in register 8 by one while we are transferring the "T", the byte address for the next character will be 317. We would later input the "h" to register 4 and when we came upon the same Indirect Transfer of the data from Register 4 to byte addressed by Register 8, we would transfer the "h" to Byte 317, etc.

4. We now have the "T" transferred into the Input Area of memory and have still retained it in Register 4. We now need to look up its escapement value. We will use an Immediate Add step to find the escapement value. As you know, the "T" in Register 4 will be in memory as a unique bit configuration. On the magnetic tape the upper case "T" appears as a 5 bit, check bit and shift bit. After going through the I/O interface, it was converted to a 3 bit and 7 bit. It will appear in memory as 01000100. Each character has its own unique bit configuration. When the machine was originally programmed, the unit spacing value of each character was installed in bytes 64 through 197. Since each character from the tape has a unique value, we can add a common quantity and come up with a second set of unique values. If the second quantity is used as an address it is possible to find the escapement value of any particular character.

Example:

MT/ST Bit Code	--8	7	6	5	4	3	2	1
Binary	128	64	32	16	8	4	2	1
'T' Code	0	1	0	0	0	1	0	0
Add 64	--	1	0	0	0	0	0	0
Total	1	0	0	0	0	1	0	0 = 132

Figure 6

The escapement value of the "T" (7 units), is located in Byte 132.

If the "h" had been in Register 4 when this step occurred we would find its escapement using the same program step.

Example:

Binary	128	64	32	16	8	4	2	1
'h' Code	0	0	1	0	0	1	1	0
Add 64	--	1	0	0	0	0	0	0
Total	0	1	1	0	0	1	1	0 = 102

Figure 7

The escapement value of the "h" (6 units), is located in Byte 102.

5. In P.S. 758 we transfer the data addressed by Register 4 to Register 10 with an Indirect Transfer step. In this case, a bump is not programmed into the program step -- Reg. 10 will now contain the escapement quantity of the "T". P.S. 760 is used to accumulate the line measure in Register 20.
6. When the operator originally set up the CCU for her job, she installed a desired line measure in memory, for instance, in Register 30. After each input character the machine must compare the accumulated line length to see if it has been filled. This is accomplished by an Arithmetic Compare Operation. (Program Step 762). In comparing the accumulated line measure (reg. 20) to the line measure set up by the operator (reg. 30), the Low and Equal latches are set according to the results of the comparison. Since the desired line measure will not be met on the first character the line measure quantity will be more than the accumulated line measure. The results of the comparison AFTER exceeding the line measure will be to set the Low latch.
7. Program Step 764 is our decision step. Have we exceeded our line measure? If we have not, Not Low will be true and step 764, Jump to Step 800 on Low, will do nothing. In other words, our program would advance to step 766. If the measure had been exceeded the Low latch would have been on and the next program step to be performed would be program step 800. The step would appear in memory as follows:

Jumps to different program steps are available for several different conditions. It is possible to jump unconditionally if desired. It is also possible to jump to a different program step or sub-routine on any condition of the Low and Equal latches.

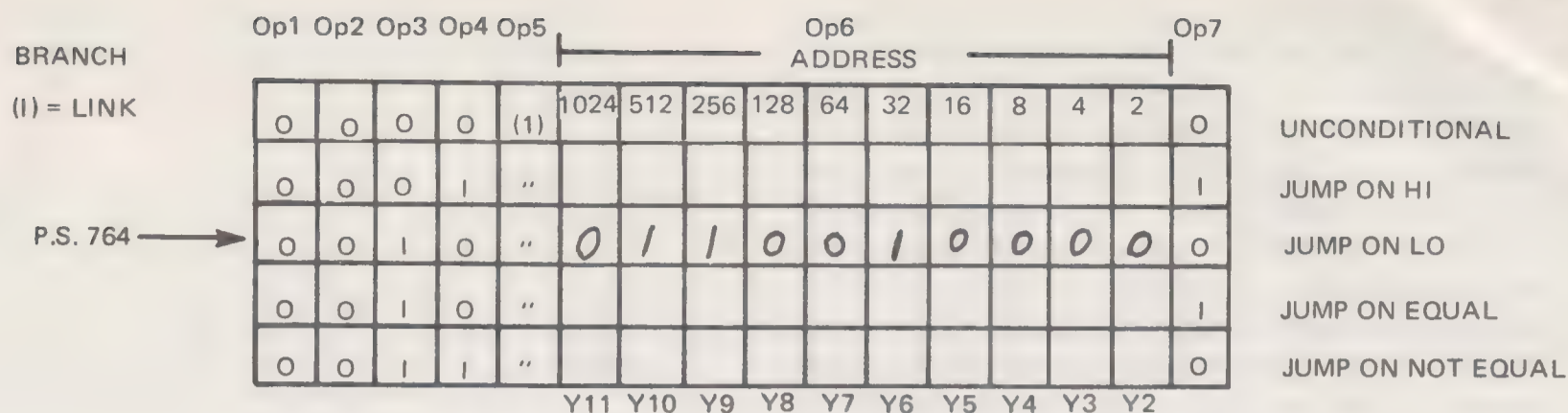


Figure 8

There are many sub-routines that must be used over and over throughout the program. The machine has the capability to jump to these routines and later return to the main program by use of a LINK. Let's use an example to explain what occurs in a JUMP and LINK operation:

Sub-routine      826 Jump Unconditional to 820  
                   824 Compare  
                   822 Add  
                   820 (Effectively Empty)

600 Unconditional Jump & Link to Step 820

Our sub-routine is located in program steps 820 through 826. Step 820 will be left empty when the machine is initially programmed. Steps 822 through 826 would be programmed as shown for this example. As we step through our main program we will finally come to Program Step 600 which is an Unconditional Jump & Link to Step 820.

This program step will cause us to jump to Step 820 and install an Unconditional Jump to step 602 instruction. In other words, link us back to Program Step 602 which is the next step to be performed after Step 600.

Sub-routine      826 Jump Unconditional to 820  
                   824 Compare  
                   822 Add  
                   820 Jump Unconditional to Step 602  
                          Installed by link

The machine would then do steps 822, 824 and 826. Step 826 is an unconditional Jump to 820. A step similar to this will be installed at the end of every sub-routine. Step 826 (Jump to 820) will cause the machine to do step 820 next. Step 820 is an Unconditional Jump back

to the next main program step 602. By having the Link always install the address of the next main program step in the first step of a sub-routine we can effectively use the routine over and over throughout the program.

- Program step 766 is an Unconditional Jump to program step 752 which is the input from the tape reader step. As you can see the unconditional jump step will be done until the line measure is filled. After the measure is filled the Jump on Low step previous to the Unconditional Jump step will be done.
- We have used almost all types of program steps. The only step not covered is the INCREMENTAL JUMP. When the MT/SC operator made her initial set-up, she made several yes or no decisions such as merge (yes or no). When she made these decisions she pushed one of two keybuttons. These keybuttons merely set or reset one bit in memory. The Incremental Jump step gives us the ability to jump FORWARD 16 program steps or BACKWARD 14 steps depending upon one particular bit condition. We can perform the jump if the sample bit is either ON or OFF. The Incremental Jump steps will appear in memory in one of the following configurations.

Only 4 Registers can contain sample bits for the Incremental Jump; however, this is an ample number of registers because 16 indicators (sample bits) can be used in each register.

- After the final calculations are made on the first line of type, the entire line would be transferred to the output allocation of memory by P and Q Indirect Transfer operations. The line would then be Outputted to the Printer through an Input-Output instruction to the Translator. The output instruction allows outputting data to either the Translator or to the Lights.

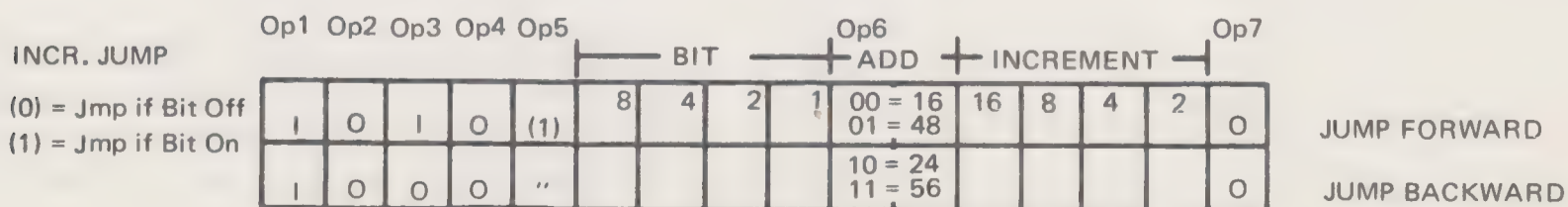


Figure 9

## PROGRAM STEP SET

IMM. ARITH.	Op1	Op2	Op3	Op4	Op5	Op6				Op7								
					ADDRESS				IMMEDIATE DATA									
	1	1	0	0	32	16	8	4	128	64	32	16	8	4	2	1		
	1	1	0	1														
	1	1	1	0														
	1	1	1	1														
					Y6	Y5	Y4	Y3										
ARITH. OPER.	Op1	Op2	Op3	Op4	Op5	Op6				Op7								
					ADDRESS 2				ADDRESS 1									
	0	1	0	0	32	16	8	4	2	0	32	16	8	4	2	0		
	0	1	0	1						0						0		
	0	1	1	0						0						0		
	0	1	1	1						0						0		
	(1) = Bump by 1	0	1	0	(1)					A1 Ind.						A2 Ind.		
(0) = No Bump	0	1	1	(1)					"						"			
					Y6	Y5	Y4	Y3	Y2					Y6	Y5	Y4	Y3	Y2
BRANCH	Op1	Op2	Op3	Op4	Op5	Op6				Op7								
					ADDRESS													
	0	0	0	0	(1)	1024	512	256	128	64	32	16	8	4	2	0		
	0	0	0	1	"											1		
	0	0	1	0	"											0		
	0	0	1	0	"											1		
	0	0	1	1	"											0		
					Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2				
INCR. JUMP	Op1	Op2	Op3	Op4	Op5	Op6				Op7								
					BIT				REG				INCR					
	1	0	1	0	(1)	8	4	2	1	00 = 16	16	8	4	2	0			
	(0) = Jmp if Bit Off	1	0	1	0	(1)					01 = 48					0		
(1) = Jmp if Bit On	1	0	0	0	"					10 = 24					0			
	1	0	0	0	"					11 = 56					0			
									Y4	Y6								
I/O INST.	Op1	Op2	Op3	Op4	Op5	Op6				Op7								
					DEVICE				ADDRESS									
	0	0	0	1	1	8 (o)	4	2	1	0	32	16	8	4	2	0		
	0	0	0	1	1	0	1	1	1	0						0		
	0	0	0	1	0	MPX (1)	0	0	0	Ind Out						0		
	0	0	0	1	0	0	1	1	1	"						0		
									Y6	Y5	Y4	Y3	Y2					
PROG. CTRL.	Op1	Op2	Op3	Op4	Op5	Op6				Op7								
					BIT				ADDRESS									
	0	0	1	1		8	4	2	1		32	16	8	4	2	1		
									Y6	Y5	Y4	Y3	Y2					
<div> <div>0</div> <div>RESET</div> <div>0</div> </div> <div> <div>0</div> <div>PRESERVE</div> <div>1</div> </div> <div> <div>1</div> <div>SET</div> <div>0</div> </div>																		

— SAMPLED —

BIT "ON" SET HI & EQUAL

BIT "OFF" SET LO & NOT EQUAL

**Figure 10**



## MEMORY LAYOUT

### MEMORY OPERATION

Writing data in magnetic core storage is very similar in many respects to recording bits on magnetic tape. To record bits on tape the record head current flows in one direction and to erase old bits from the tape the record head current flows in the opposite direction. The tape after being recorded contains magnetic flux paths of opposite polarities. We arbitrarily call the magnetic flux paths recorded in one direction a "bit" or "one" and magnetic flux recorded in the opposite direction "blank" or "zero".

A magnetic core storage memory is composed of many small donut shaped ferrite cores. The magnetic flux paths of a core can be reversed so that it is magnetized in one direction or the other. Just like magnetic tape, we can arbitrarily select one direction of magnet flux to be called a "bit" or "one" and the other direction of magnetic flux to be called "blank" or "zero."

Instead of reversing record head currents above a magnetic tape to record bits we merely need to pass currents through wires that go inside the magnetic cores to record bits. A 400 ma. current is required to change the state of the cores in the Composer Control Unit's memory. If 400 ma. is passed through a core as shown in Fig. 1A, we can arbitrarily say that we have recorded a "bit" or "one". If 400 ma. is passed through the

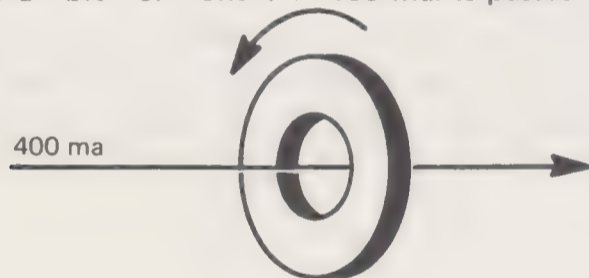


Figure 1A

core in the opposite direction, as shown in Fig. 1B, we can say that a "zero" has been written into the core. Once a "one" or "zero" has been written into a core it will stay there until changed. Although 400 ma. of current is the force needed to



Figure 1B

change the state of a core, the 400 ma. does not necessarily have to come from one source, i.e., 200 ma. flowing through each of two wires will accomplish the same job (Fig. 2). If 200 ma. were flowing in only one of the two wires the core would not be changed. This is called a HALF-SELECT. If the currents were flowing through the two wires in opposite directions, the effects of the currents would cancel and the core would not be affected.

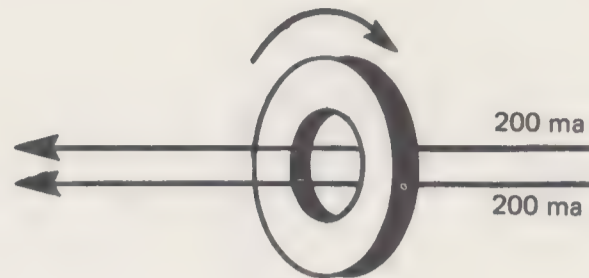


Figure 2

It is not necessary to have the wires go through the core in a parallel configuration. The wires could go through the cores as shown in Fig. 3A or 3B. As long as the current forces work in the same direction, the core can be changed.

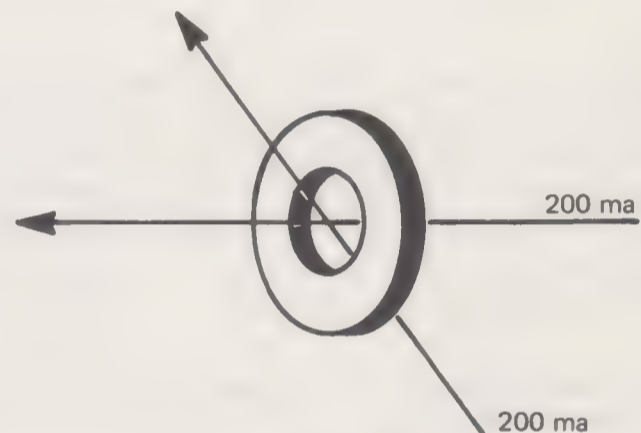


Figure 3A

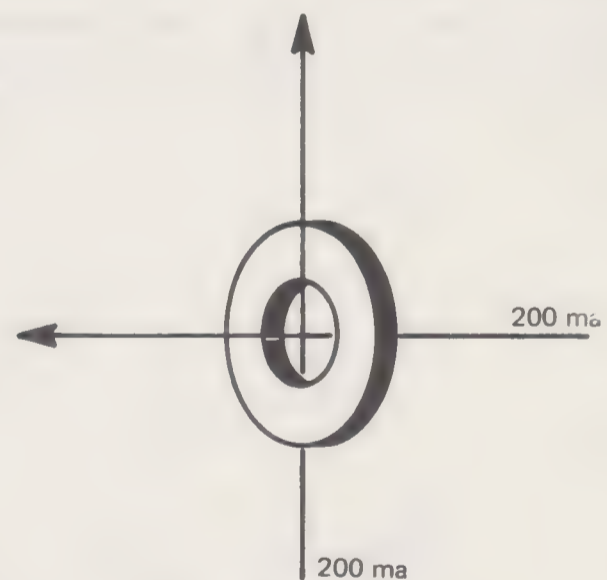


Figure 3B

In order to read a bit that has been recorded in a core, it is necessary to pass a THIRD WIRE through the core. This third wire is a SENSE LINE. Let's assume that the necessary 400 ma. write current has been passed through the core and that a "one" has been recorded in the core. To read the core, the currents in the two wires that were used to write the "one" are reversed. The currents will now cause the core to revert back to a "zero" state. When the core changes state a small AC voltage is induced by the flux change that takes place with the polarity shift. This AC voltage is induced in the sense wire by transformer action. The signal induced in the sense line is

amplified so that it can be used as a logical signal in the processor. If the core had not contained a "one" no polarity change would have taken place; therefore, no flux change would be available to induce a signal into the sense wire (Fig. 4).

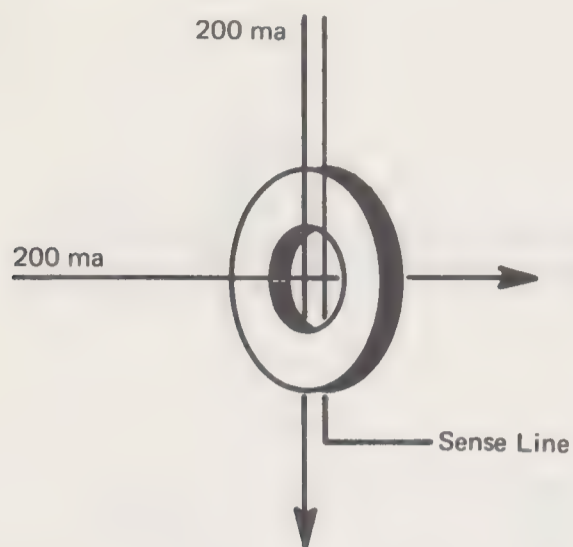


Figure 4

You have seen that by passing 200 ma. currents through each of two wires in one direction, we can write a bit into a core. Let's call the currents flowing in this direction WRITE CURRENTS. You have also seen that by reversing the 200 ma. currents through the two wires the core is read using a sense line. The currents flowing in the read direction are called READ CURRENTS. All cores read are left in a "zero" state.

It is apparent that in order to record useful data, "one's" must not be recorded in every core.

Usable information must contain "zero's" and "one's". In order to record a "zero" in a core, all that is necessary is to prevent the core from changing state when the write currents occur. During write time, the sense amp circuits are turned off

and the sense lines are used as INHIBIT LINES. They are called inhibit lines because when active they prevent writing a "one" in the core where we want a "zero". The sense inhibit line runs parallel to one of the lines that will pass 200 ma. of write current. To prevent writing "one" into a particular core at write time a 200 ma. current flow will occur in the inhibit line in the OPPOSITE direction of the current flowing in one of the write lines (Fig. 5). The current flowing in one of the write lines and the current flowing in the inhibit line oppose each other so that the resultant current through these two lines cancels. The 200 ma. flowing through the second write wire is insufficient to change the state of the core. Therefore, the core is left in a "zero" state. The inhibit currents are controlled by the current source logic discussed in machine organization.

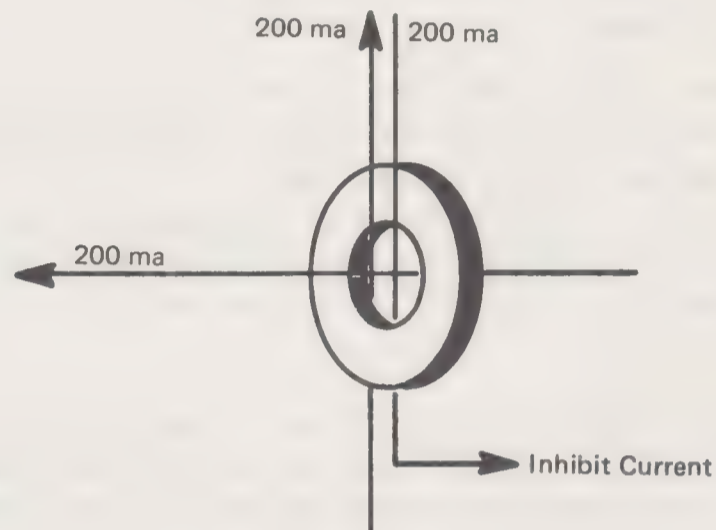


Figure 5

To fully utilize the memory wiring many cores are strung on each wire. The only cores affected by write or read currents are those intersected by two parallel 200 ma. current forces (Fig. 6).

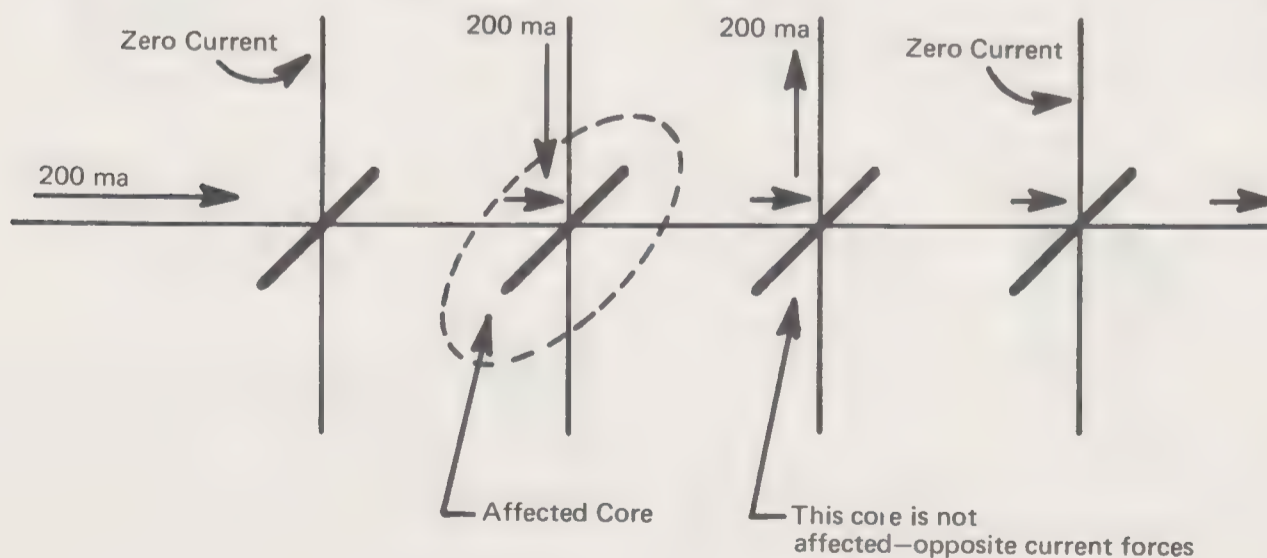


Figure 6

The memory in the CCU is designed to operate upon 4 cores or four bits at a time. The two lines required for reading and writing data into memory are called X and Y lines. An X DRIVER and X SWITCH is used to control one Read/Write line while a Y DRIVER and Y SWITCH is used to control the other. Both X and Y Drivers and switches, have the ability to allow current to flow in either direction. The current flow through the X lines is controlled strictly by gates for reading and gates for writing. READ CURRENTS flow from the X Driver to the X Switch when the Clock selects READ TIME. During WRITE TIME the current flows from the X Switch to the X Driver (Fig. 7).

The Y Drivers and Y Switches are controlled by read and write gates and also by gates to divide each byte of memory into

two groups of four cores (even cores and odd cores). One byte from memory showing only Read/Write lines is illustrated in Fig. 7. During each Instruction Time cycle there are four bit time cycles (machine organization section). During each BIT TIME cycle FOUR cores are operated upon from each of two different memory locations. For the moment let's look at the operation of the lines for only one location in memory. During the first bit time the Clock will generate signals that will gate the X Drivers and X Switches for read current flow. The Clock will generate additional signals causing the Y Driver and Y Switch currents to flow in a READ EVEN direction (Fig. 8A). Only the cores that have current forces occurring in the same direction will be affected. Had "ones" been recorded in any of the cores, the core/cores would have been reset to "zero". The sense lines (not shown in Fig. 8) would have detected bits as the cores changed state (flipped).

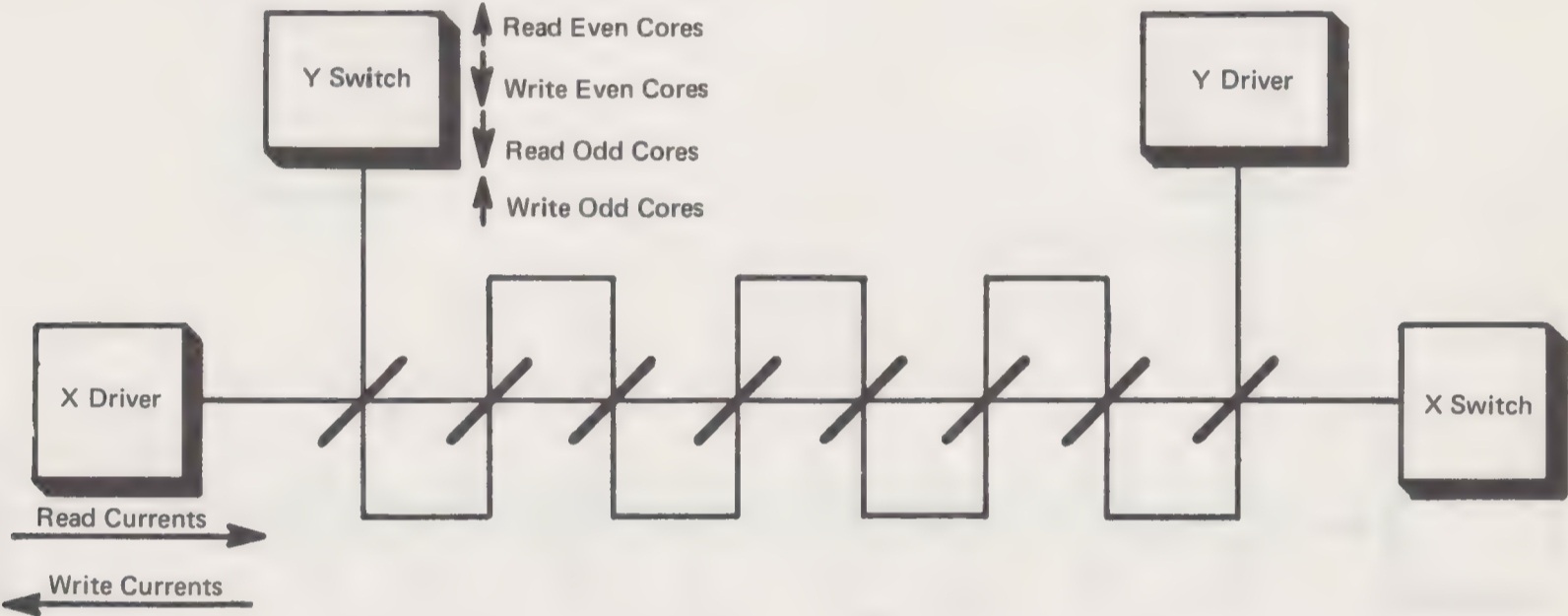


Figure 7

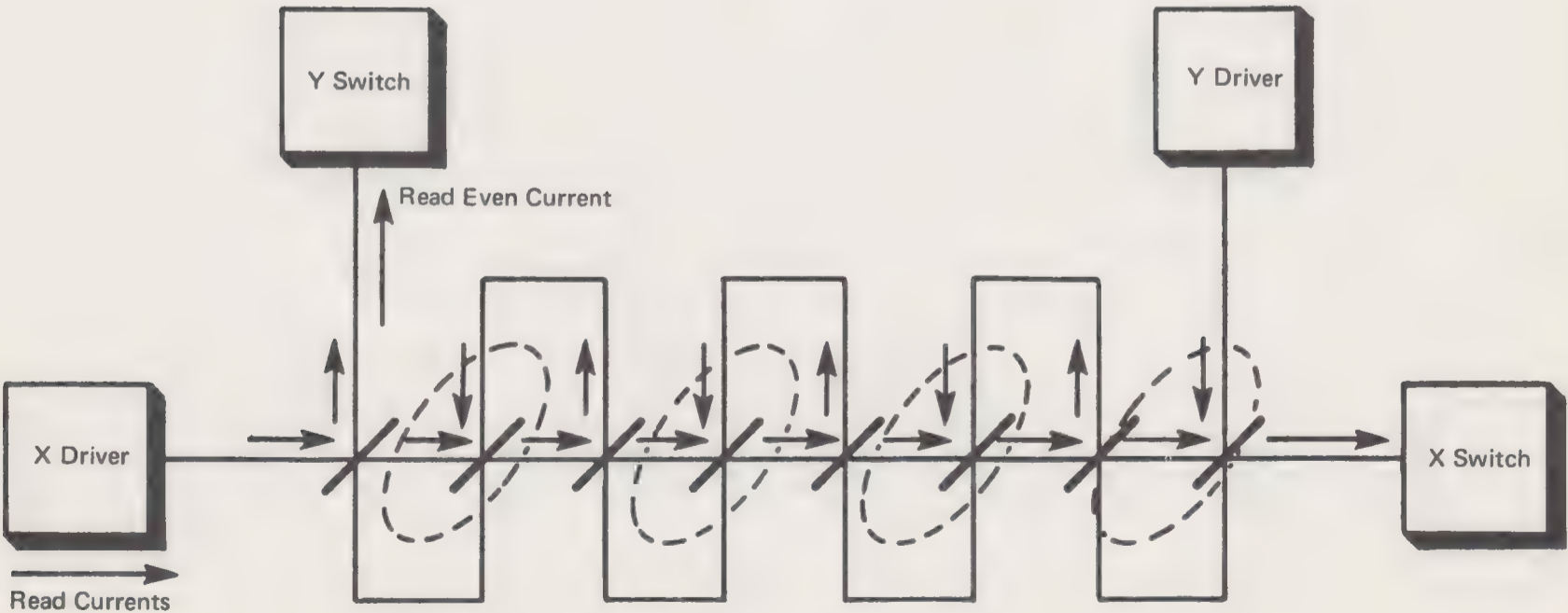


Figure 8A - Read Even Cores

"zero" state and any bits read would be detected by the sense line circuitry. When it becomes time to write back into the odd cores both X and Y current directions are reversed and the same four cores will be written (Fig. 9B).

During each Instruction Time cycle 4 bit time cycles occur. During the 1st and 2nd bit times the afore-mentioned sequence occurs. During the 3rd and 4th bit time the same sequence occurs using a different Y line.

Note, current flowed in the Y lines in the same direction for both reading the even cores and writing the odd cores. Likewise, the current direction was the same for both reading the odd cores and writing the even cores. The clock signals controlling the gates to the Y Drivers and Y Switches are named READ EVEN — WRITE ODD and READ ODD — WRITE EVEN. Clock signals gating the X Drivers and Switches are merely named READ and WRITE.

The next portion of the bit time cycle would be to WRITE data back into the SAME FOUR CORES. Clock signals generated for this first cycle would define write the even cores. A current flow reversal takes place in both the X and Y lines. If Inhibit lines were present we would be able to inhibit writing "ones" in the cores that should contain "zeros". For illustration no inhibits are used (see Fig. 8B). The four even cores that were previously read will be affected by the combined 400 ma. flowing through them. The four even cores will now contain "ones". During the next bit time the clock will generate signals to define a READ ODD core cycle. The read signals will cause read currents to again flow from the X Driver to the X Switch. However, the current from the Y Driver to the Y Switch will not change direction from the previous write even cycle. By changing direction of current flow in only the X lines, four other cores are selected to be read. This second group of 4 cores are called the ODD CORES (Fig. 9A). The selected cores that contained "ones" would be flipped to a

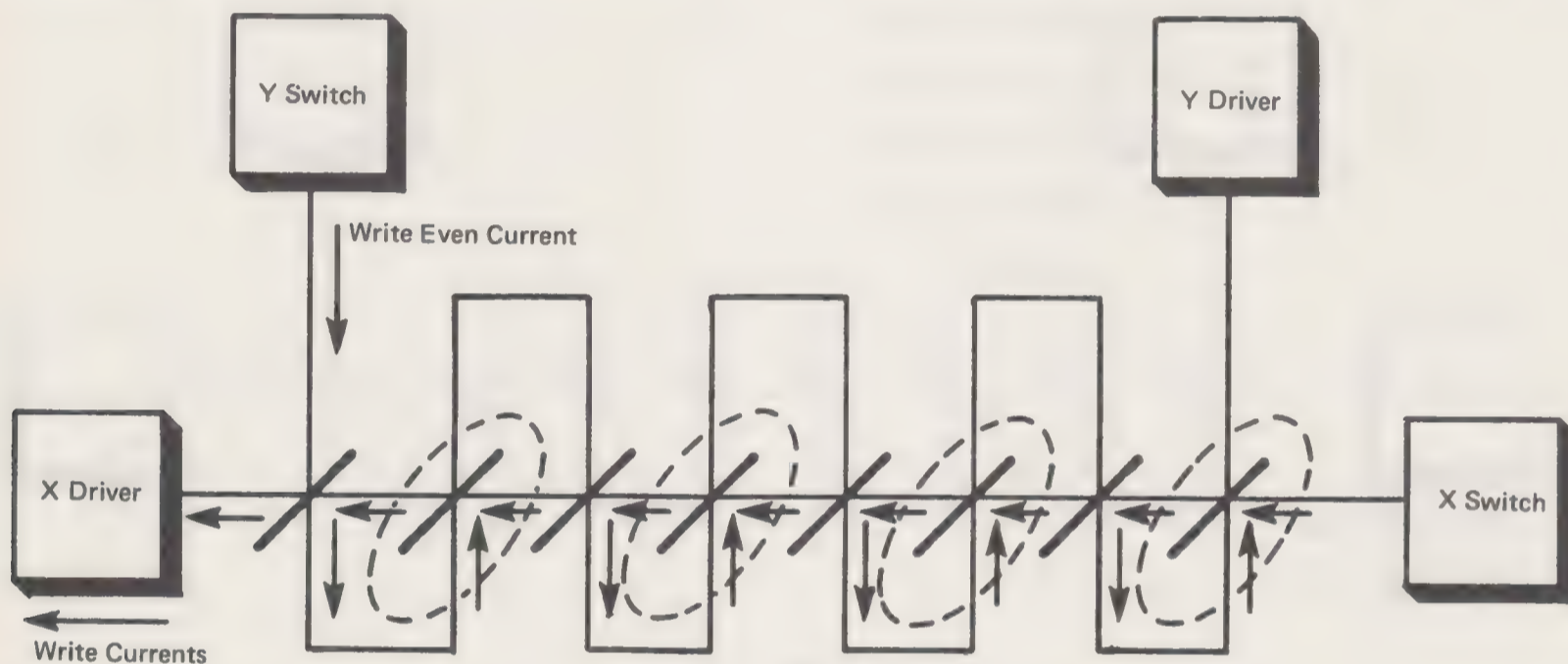


Figure 8B - Write Even Cores



Figure 9A - Read Odd Cores

The CCU uses 8 X Drivers and 8 X Switches in conjunction with 8 Y Drivers and 4 Y Switches for making selections of desired cores in memory. Each X Driver has 8 wires attached. One of these wires goes to each of the 8 X Switches. Since there are 8 X Drivers it is apparent that each X Switch also has 8 wires attached (Fig. 10). A total of 64 X lines go through memory. For current to flow in any one of these X lines we merely select any combination of an X Driver and X Switch.

Each line passes through 32 bytes in memory.

Each Y line intersects one byte (8 cores) on each of the 64 rows of cores strung on the X lines. Each Y Driver has 4 wires which are dispersed to each of the Y Switches. A total of 32 Y combinations are available. By selecting a combination of one X Driver, one X Switch, one Y Driver, one Y Switch, and by gating the current direction, any 4 cores in memory can be read or written.

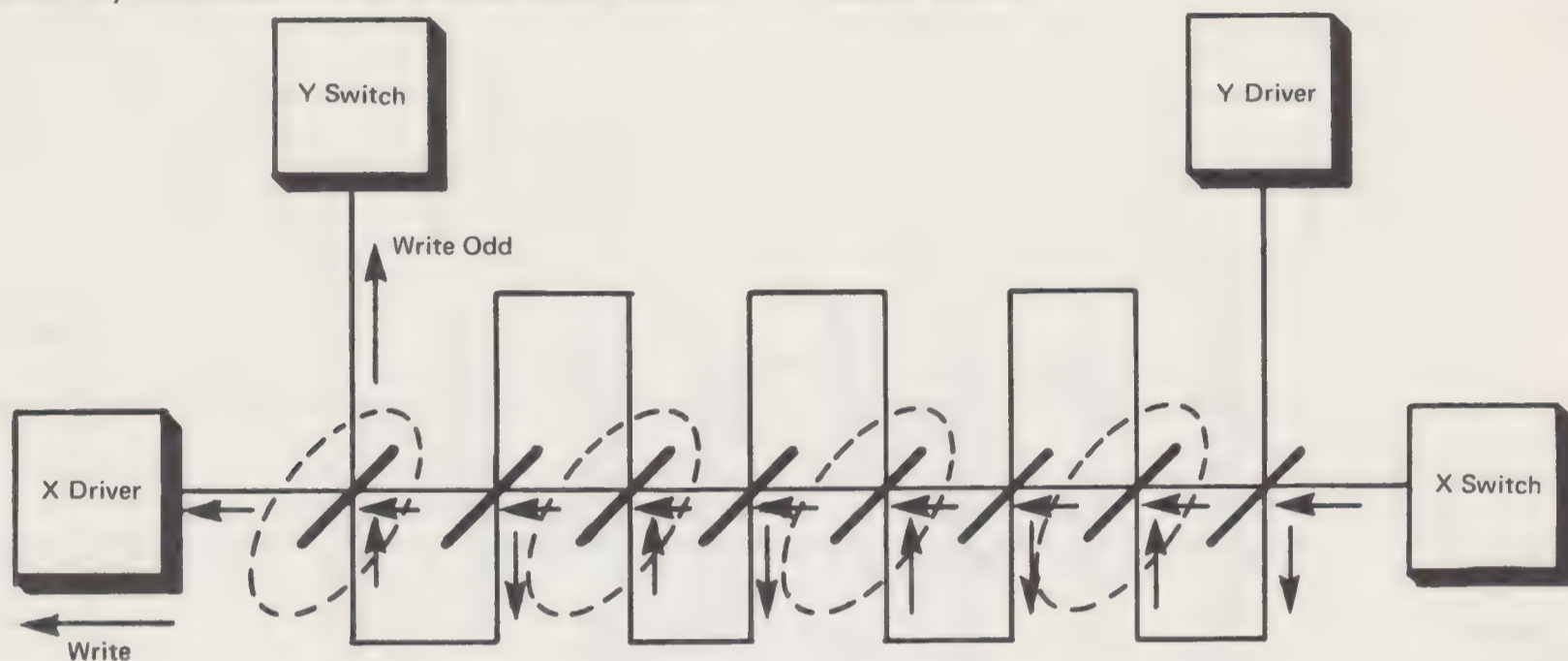


Figure 9B - Write Odd Cores

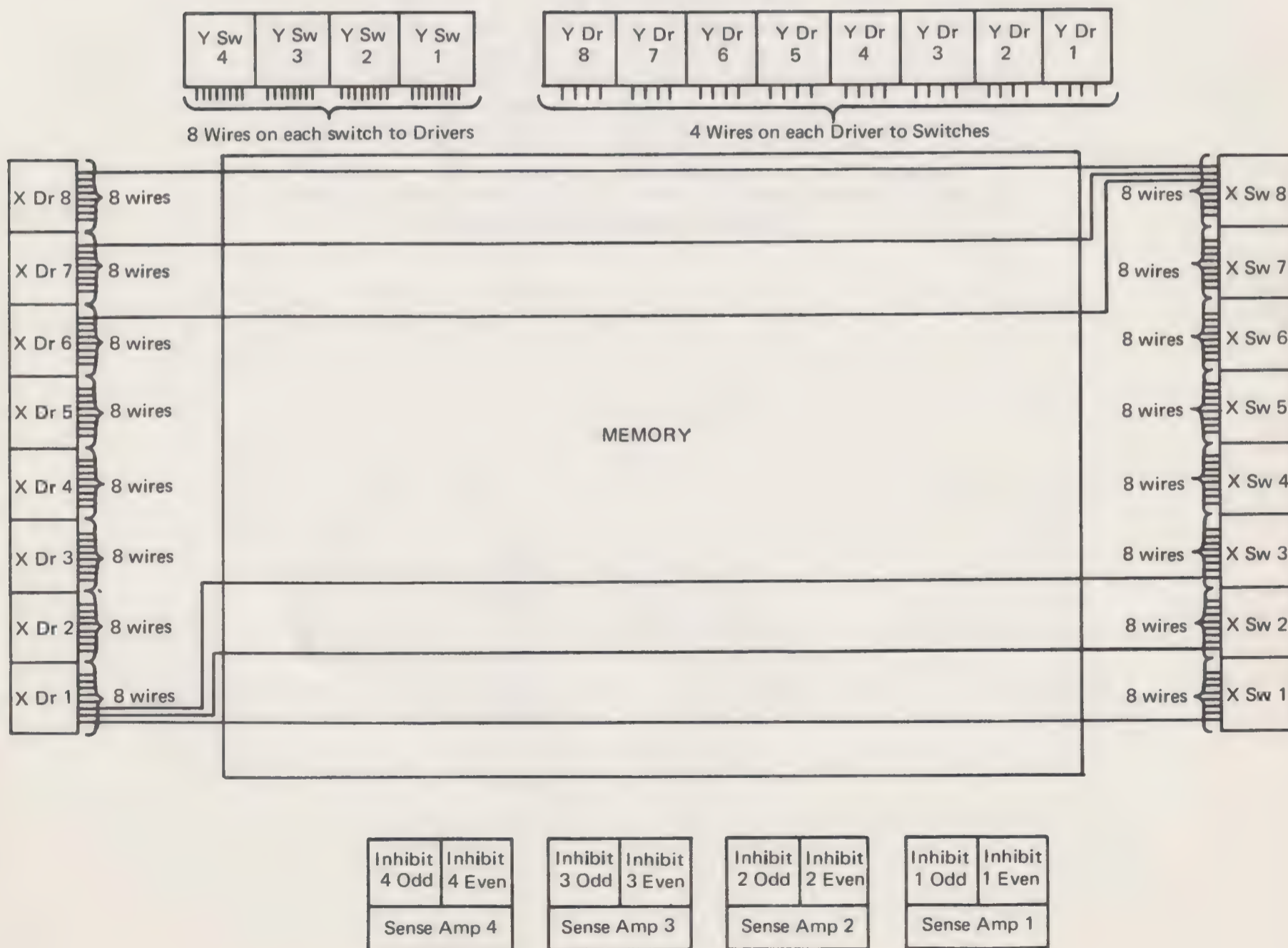
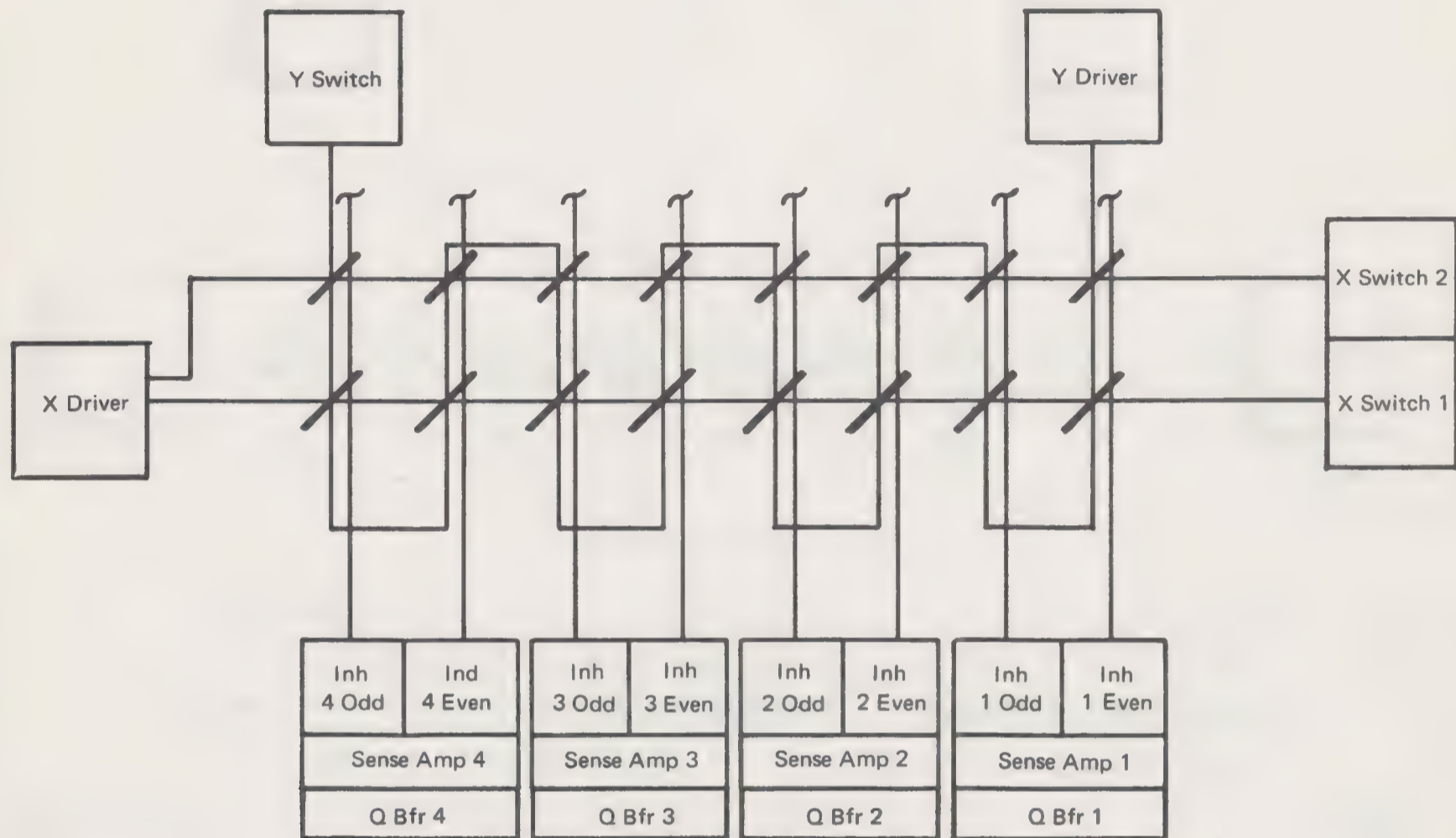


Figure 10 - Lines to Memory

In addition to the X and Y lines a Sense Inhibit line goes through each core in memory. There is one line for each of the 8 bit positions in each byte (Fig. 11). The Inhibit lines are divided into odd and even groups so that the current flowing from the Inhibits will oppose that flowing in the Y lines while writing. While reading, the INHIBIT function of the lines become SENSE LINES. The 8 Inhibit lines become effectively 4 Sense lines due to internal coupling of the sense amp/inhibit

circuits. The four Sense Amps amplify the bits read at read time and the bits then set the Q Butter. At write time the inhibit functions of the circuits are allowed to become active. If a "one" is to be written into a bit position, inhibit currents for that position will remain off. If the bit position is to remain in a "zero" state (flipped to zero when read), the inhibit line for that position will turn on and oppose the Y write currents. The inhibit circuits are controlled by 4 current sources in the processor and by the Clock.



**Figure 11 - Sense/Inhibit Lines**

## CLOCK CIRCUITS

### PURPOSE

To provide timing pulses in the CCU a 17 latch counter is used. The latches are driven by a 240KC crystal oscillator whose output drives a binary trigger. The trigger drives two out of phase single shots called SSA and SSB. The duration of each SSA and SSB is 2.4 microseconds.

The purpose of these basic driving pulses and the latches which they drive is to generate signals to define primary times to control machine operation. These times are Memory Cycle, Bit Times, and Instruction times. We will discuss each of these times — seeing how they are generated and their primary purpose during each CCU cycle.

### MEMORY CYCLE COUNTER

The memory cycle counter consists of a binary counter whose output signals are called A and B and a trinary counter whose output signals are called TIME WRITE, P TIME, and CENTRAL BIT TIME. The signals generated by the memory cycle counter will be used to define two read times, two write times and steering pulses which are used to control other pulses and resets. It will be important to understand that in electronic circuits the absence of a specific signal may be (and usually is) just as important as the presence of that signal. This may be noted in the following description of the signals and their uses: SSA and SSB are used as basic timing pulses and also as controls for the duration of Y Currents. Signals A and B are used to control the X and Inhibit Currents. These are the currents which are used to read and write in memory. The Time Write signal defines the WRITE TIME of the memory cycle while Not Time Write (written —TIME WRITE) defines READ TIME. The P Time signal identifies P TIME while —P TIME identifies Q TIME. The Central Bit Timing signal is used to steer (or control) Time Write and to provide a timing pulse to control reset signals.

Summarizing the above we find that the basic oscillator pulses are expanded through trigger and latch circuitry to provide pulses which will be used to define times in each cycle of the Clock. These times in turn have given us definition of:

P Time  
Q Time  
Read Time (Read P and Read Q)  
Write Time (Write P and Write Q)

Referring to the Clock timing chart it will be seen that the sequence of development of these times are Read P, Read Q,

Write Q and Write P. In other words, considering an address of memory, we could now read one bit group of ferrite cores of the P address, read one group of cores of the Q address, write back into the Q address cores, and then write back into the P address cores. The total Clock time needed for this bit cycle is 50 microseconds.

During certain bit times it will not be necessary to address two memory locations. Only one register will be addressed and this is done during P Time. This is called a P ONLY CYCLE. By adding another signal (P only) to our Clock logic the clock circuits are conditioned to omit the Q Read Time. The P Only cycle is useful when we want to read data from one memory location, write it into another memory location, and rewrite it back from whence it came. The bit time is also reduced from 50 microseconds to 33.3 microseconds.

During each Read-Read/Write-Write sequence we are able to address four bits from each of two memory locations. This cycle is called a BIT TIME. Each register area in memory consists of 16 bits. Since we are addressing only 4 cores in each register during a Bit Time it is necessary for the Clock to define four Bit Times for a complete address of each register. With this in mind, let us look at the next Clock circuit which will generate these four Bit Times for us.

### BIT TIME COUNTER

As previously stated, the Bit Time counter will be used to generate signals which will define four Bit Times. These signals are the outputs of two pairs of latches. The output of one pair of latches provides signals called BIT COUNTER A and BIT COUNTER B while the other pair provide signals called STEER BIT COUNTER A and STEER BIT COUNTER B. The two steering latches provide control to the two Bit counters. Bit Counter A and Bit Counter B will be used in combinations to produce four BIT TIMES called Bit 1/4, Bit 5/8, Bit 9/12, and Bit 13/16. The chart below shows how the combinations of the Bit Counters may be used to define Bit Times.

—Bit Ctr A and —Bit Ctr B = Bit 1/4  
Bit Ctr.A and —Bit Ctr B = Bit 5/8  
—Bit Ctr A and Bit Ctr B = Bit 9/12  
Bit Ctr A and Bit Ctr B = Bit 13/16

Here again may be noted the importance of "Not" signals and how they are used to provide additional circuit conditions. By considering not only the presence of a signal (Bit Counter A for instance) but also the absence or off condition of that same signal, we are able to use only two signals Bit Ctr A and Bit Ctr B to provide four timing conditions.

With the signals which the Clock has generated up to this point, we are able to address two complete registers in memory. We now have the ability to Read and Write four Bits at a time for four Bit times, i.e., Bits 1/4, Bits 5/8, Bits 9/12, and Bits 13/16.

INSTRUCTION TIME COUNTER

The Instruction Time Counter will generate signals which will define machine INSTRUCTION TIMES. In order for the CCU to perform the necessary functions for the different program steps there must be a maximum of ten Instruction Times. However, all ten Instruction Times are not necessary for every program step. Therefore, additional signals must be provided to condition the Clock circuits to not only progress from one Instruction Time to the next but also to permute from – let’s say Instruction Time 1 to Instruction Time 6. At the end of the tenth “I” Time the counter must be returned back to the beginning time, called Instruction Time Zero, so that it will be ready for the next program step.

The “I” Time Counter consists of four indicator latches called INSTRUCTION TIME COUNTER A, B, C, and D. To control the progression or skipping of the Indicator latches four steering latches are used. These are named STEER INSTRUCTION CRT A, B, C, and D. Steering latches are used in this manner because we have the ability to change the Steering latches at some time during the cycle without a corresponding change to the Indicator latches. The Steering latches merely set up logic to change the Indicator latches at the proper time. By this means we can make the Clock circuits permute from one “I” Time to the next one that is required. During a cycle that requires all ten available Instruction Times we step from Insn 0 to Insn 1 to Insn 2, etc. up through Insn 9 time. The various permute combinations needed are:

- Insn 1 to Insn 0, 6, 9
- Insn 2 to Insn 5
- Insn 3 to Insn 0, 6, 9
- Insn 5 to Insn 0
- Insn 6 to Insn 9
- Insn 9 to Insn 0

The chart below shows how the four Instruction Time Counters, Instruction Counter A (IA), Instruction Counter B (IB), Instruction Counter C (IC) and Instruction Counter D (ID), may be used to define ten Instruction times.

Insn Time	8	4	2	1
0	= − ID − IC − IB − IA			
1	= − ID − IC − IB	IA		
2	= − ID − IC	IB − IA		
3	= − ID − IC	IB	IA	
4	= − ID	IC − IB − IA		
5	= − ID	IC − IB	IA	
6	= − ID	IC	IB − IA	
7	= − ID	IC	IB	IA
8	=	ID − IC − IB − IA		
9	=	ID − IC − IB	IA	

NOTE: The Instruction Counters have a direct binary relationship to the Instruction Times defined by the counters.

CLOCK PULSE DEVELOPMENT

When power is supplied to the console, the Crystal oscillator starts running. The oscillator drives two single shot circuits which produce alternate 2.4 microsecond pulses recurring every 8.3 microseconds. These signals are called SINGLE SHOT A (SSA) and SINGLE SHOT B (SSB).

SSA and SSB in turn drive a binary counter whose outputs are signal A and signal B. The outputs of A and B are used to control each other with SSA and SSB providing the other control.

A is set anytime SSA is true, provided B is NOT true (reset). A is turned off (reset) on each SSA if B is on (set). B is set on each SSB if A is set. B is reset on each SSB if A is off (reset).

We now have four signals being generated continuously as long as the oscillator is active; SSA, SSB, Signal A and Signal B. It can be seen that A will follow SSA and B will follow SSB, i.e., Signal A sets on one SSA and resets on the next SSA while Signal B sets on one SSB and resets on the next SSB.

Note that after power is applied the oscillator remains active, but SSB can be stopped by using the Clock Control Switch.

The A and B signals are used to drive a trinary counter which consists of three latches. The outputs of these three latches are Time Write, P Time, and Central Bit Time.

The output TIME WRITE will control the read and write currents in the machine cycle. If Time Write is set we are in WRITE time; if Time Write is reset we are in READ time.

The output P TIME will control the data addressed in memory. If P Time is set the memory location defined as the P TIME register will be addressed. If the P Time latch is reset, the memory location defined as the Q TIME register will be addressed. Data read at P Time will be stored in the P TIME BUFFER while data read at Q Time will be stored in the SENSE AMP TRIGGERS (effectively the Q Time Buffer).

The output CENTRAL BIT TIME is used to steer the setting and resetting of Time Write and P Time and is also used to control reset timing and central timing pulses.

TIME WRITE may be set by two separate conditions. During a P ONLY cycle Time Write will set when signal A is down and Signal B, Central Bit Time, and P Only are up. The P Only signal is up when we need to read data from only one memory location. The other set conditions for Time Write (regular P and Q cycle) are: –A, B, –Central Bit Time, and –P Time. In either cycle Time Write is reset by a pulse called Reset Indicators.

The signal Time Write can now be used in conjunction with A and B to generate another signal called STEERING LATCH STROBE. The turn on conditions for Steering Latch Strobe are  $\neg A$ ,  $\neg B$  and Time Write. This circuit is not a latch and will remain true only as long as all three of its inputs are true. Steering Latch Strobe will be used to control the Bit Times and Instruction Times.

P TIME is controlled by the Binary Counters A and B and by the output of Time Write. The set conditions for P Time are A,  $\neg B$ , and Time Write. P Time is reset by a signal called Bump Strobe Time which will be discussed later.

CENTRAL BIT TIME is controlled by the Binary Counters A and B and by the other two outputs of the trinary counter P Time and Time Write. The set conditions of Central Bit Time are: A,  $\neg B$ ,  $\neg TW$  and P Time. Central Bit Time will set at P Read Time when A is set and B reset. Central Bit Time will reset on the next A and  $\neg B$  condition when either Time Write comes true or P Time becomes false.

Previously it was mentioned that Central Bit Time was used to control resets and central pulses. First, let's consider the central pulse called Bump Strobe Time.

BUMP STROBE TIME is used to reset P Time. Therefore, any time P Time becomes true we will remain in P Time until Bump Strobe resets the P Time latch. Bump Strobe is used to change the machine timing from P to Q Time. The turn on conditions for Bump Strobe are:  $\neg A$ , B, and Central Bit Time. Since the circuit is not a latch, Bump Strobe will remain on only as long as its three conditions are satisfied.

The reset signal controlled by Central Bit Time is called RESET INDICATORS. Like Bump Strobe, it is not a latch. The turn on conditions for Reset Indicator occurs during P Time with Central Bit Time untrue for the duration of SSA, which is the shortest of its input signals. This short duration pulse is used to reset the Indicator Latches which in turn are used to define Instruction Times and Bit Times in the CCU operation.

The LOAD INDICATOR signal occurs during the same time period that the Reset Indicator signal is true. Load Indicator comes true at  $\neg A$ , B, P Time. Since the steering latches are the prime controlling factors for setting Indicators, the fact that both the load and reset signals occur simultaneously is of no consequence. The Indicator Latches will always follow the Steering Latches when the set and reset signals occur together (set overrides reset).

To identify bit times four latches are used. Two of these latches generate steering pulses. These signals in turn control two bit time indicator latches called BIT TIME COUNTER A and BIT TIME COUNTER B. The set and reset condition for these latches is as follows:

Set Steer Bit Ctr A =  $\neg$ Bit Ctr A and Steering Latch Strobe.  
Reset Steer Bit Ctr A = Bit Ctr A and Steering Latch Strobe.

Set Steer Bit Ctr B = Bit 5/8 and Steering Latch Strobe  
Reset Steer Bit Ctr B = Permute Time

Set Bit Time Ctr A = Steer Ctr A and Load Indicator.  
Reset Bit Time Ctr A = Reset Indicator.

Set Bit Time Ctr B = Steer Bit Ctr B and Load Indicator.  
Reset Bit Time Ctr B = Reset Indicator.

The Instruction Times are identified by four latches, i.e., Instruction Time Counters A, B, C and D. These indicators in turn are controlled by four steering latches called STEER INSTRUCTION TIME COUNTER A, B, C and D. The set conditions for the Instruction Time Counters are controlled by a signal called LOAD INDICATOR and the outputs of the Steer Instruction Time Counter latches. The set conditions for Load Indicator Time Counter have already been covered. The Steer Instruction Time Latches have many conditions for setting. Basically the set conditions will follow a signal called PERMUTE INSTRUCTION TIME STEERING LATCHES anded with conditions of the Instruction Time Counters, Bit Times, Operational Codes and Jump signals as dictated by the particular operation being performed by the Processor. With these various conditions controlling the steering latches we have the ability to progress sequentially from Instruction Time 0 through Instruction Time 9 or to PERMUTE (skip) several Instruction Times ahead in order to perform the instructions called out by the Processor program. We cannot permute backwards except to I-0 Time when we want to begin another series of Instruction Times.

Once the Instruction Time Counters are set they will remain set until RESET INSTRUCTION TIME STEERING LATCHES comes true. The conditions to bring up this reset are: SSA, B, P Time and  $\neg$ Central Bit Time.

Once the Steer Instruction Time Counters have been set they will remain set until RESET INSTRUCTION TIME STEERING LATCHES comes true. There are several conditions for bringing this signal up; however, it will generally follow the signal STEER LATCH STROBE and PERMUTE INSTRUCTION TIME STEERING LATCHES plus conditions of the Instruction Time Counters. Steering Latch Strobe is conditioned by  $\neg A$ ,  $\neg B$  and Time Write.

Specific conditions to control the permute signals will be covered in more detail later under their appropriate sections.



## MEMORY ADDRESS LOGIC

### INTRODUCTION

The logic required to address desired memory locations is controlled by Memory Address Latches and Clock signals. The very first thing that must be accomplished by the CCU in any mode of operation is to find the address of the program steps to be done.

The address of the program step is located in the special area of memory allocated for this purpose. The PROGRAM STEP ADDRESS REGISTER will be addressed by the Clock alone. The program step address is read from memory during the first Instruction Time, named I-0. With the Clock in I-0 time it will perform P ONLY memory cycles. During each of the four bit times the Clock will define a Read P Time, Write Q Time, and Write P Time. During the entire I-0 Time the memory drivers and switches will be gated to operate on the cores in the program step address portion of memory. The clock time indicator latches (Instruction Time Counters A, B, C, and D) are all down at I-0 time. The not signals from these latches are anded together to generate a clock signal named I-0. The I-0 signal is used to turn on a circuit called SELECT PROGRAM STEP ADDRESS in the memory allocation logic. Memory allocation logic will in turn control the MA DECODE (machine organization).

Memory allocation logic is composed of 6 circuits. Four circuits are used to select special memory addresses while the remaining two circuits are used to select memory locations outside the special area. The four circuits used to select the special addresses are named: Select Program Step Address, Select A-Word, Select B-Word, and Select Special (Fig. 1).

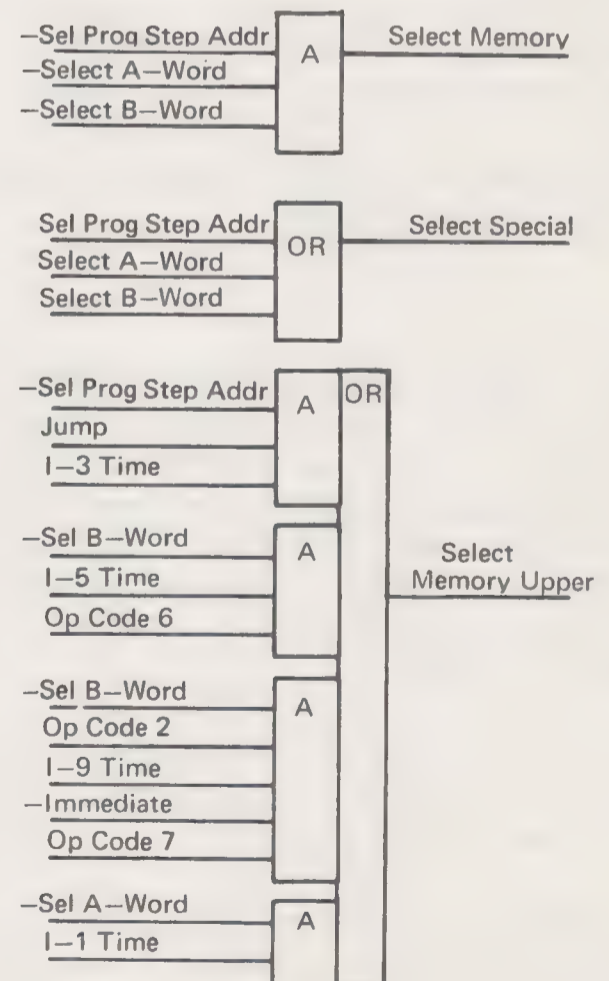
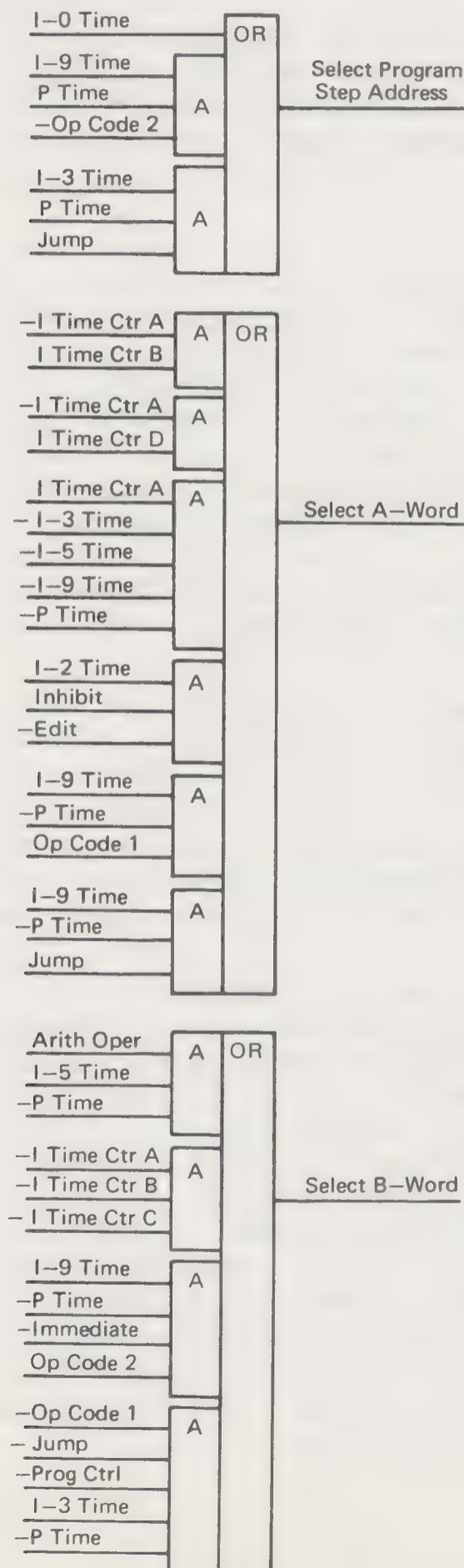


Figure 1 - Memory Allocation Logic

Select Program Step Address, Select A-Word, and Select B-Word are turned on by clock signals and/or in conjunction with signals generated by the Operational Code Latches. SELECT SPECIAL is turned on if any of the three special addresses are on. If none of the special addresses are true the SELECT MEMORY signal is up. Select Memory is true when any portion of memory other than the special area is to be addressed. SELECT MEMORY UPPER is controlled by clock signals in conjunction with operational codes and signals generated by the operational codes. Select Memory Upper is true for addresses in the area of memory above the low order working registers. Select Memory and Select Memory Upper both must be true to address a memory location above the low order 32 registers. If a low order register is to be addressed Select Memory alone can control the MA decode for selection of the proper cores, i.e., Select Special, Select Memory, and Select Memory Upper defines general allocation logic while Select Program Step Address, Select A-Word, and Select B-Word define registers in the special allocation.

As previously mentioned, in I—0 time the Select Program Step Address circuit will become active. Select Program Step Address can be turned on at times other than I—0 time for particular operations, but at the beginning of a machine cycle the type operation to be done is unknown. Therefore, the clock time I—0 alone activates the circuit. When Select Program Step Address becomes true, Select Special is turned on and Select Memory is turned off (Fig. 1). Throughout the I—0 cycle the outputs of the memory allocation circuits will be:

Select Program Step Address	-	Up
Select A-Word	-	Down
Select B-Word	-	Down
Select Special	-	Up
Select Memory	-	Down
Select Memory Upper	-	Down

With these outputs in mind, let's proceed into the logic used in the Memory Address Decode.

## LOGIC

The Memory Address Decode logic is used to supply gates for the various X and Y Drivers and Switches so the proper cores in memory can be read and written at the proper times. There are four groups of decode circuits. One group is used to select X DRIVERS, one group selects the X SWITCHES, another group selects the Y DRIVERS, and the fourth group selects the Y SWITCHES. There is a total of 14 circuits used in the Memory Address Decode logic.

The X Driver decode inputs come from general memory allocation logic and from three Memory Address Latches whose outputs are named Y8, Y9 and Y10.

If Select Memory is up while Select Memory Upper is down, Decode X Driver 1 will turn on (Fig. 2A). If Select Special is up Decode X Driver 8 will turn on. All other inputs to the X Drivers can only be satisfied if Select Memory Upper is true. If Select Memory Upper were true the Decode X Driver cir-

cuits selected would depend upon the condition of Y8, Y9, Y10 combinations. In effect we are ignoring the Y8, Y9, and Y10 Memory Address Latches unless Select Memory Upper is true.

The X Switch Decodes are selected by general memory allocation logic and by Memory Address Latches Y4, Y5, and Y6. If Select Special were true Decode X Switch 8 would be chosen (Fig. 2B). All other Decode X Switch logic requires only that Select Memory be true. Since Select Memory will be true for any memory address outside the special allocations we will decode Y4, Y5, and Y6 combinations for any general memory operation.

To select the proper Decode Y Driver circuits we use both general and specific memory allocation logic in conjunction with Y2, Y3, and Y11. If Select Memory is up and Select Memory Upper is down, Decode Y Driver 1, 2, 3, 4 will be activated. It is also possible to select combinations of the other three Decode Y Driver circuits depending upon the conditions of Y2, Y3, and Y11.

If Select Special is true Decode Y Driver 2, 4, 6, 8, Decode Y Driver 3, 4, 7, 8 and Decode Y Driver 5, 6, 7, 8 will be selected. The combination of outputs from the three Decode Y Driver circuits depends upon which of the special allocation addresses is selected. If the Select Program Step Address signal was up in the memory allocation logic (Select Special would be true) all three of the aforementioned Decode Y Driver circuits would be true. If the Select A-Word signal were true, Decode Y Driver 3, 4, 7, 8 and Decode Y Driver 5, 6, 7, 8 would be true. If Select B-Word were true Decode Y Driver 2, 4, 6, 8 and Decode Y Driver 5, 6, 7, 8 would be true.

The Decode Y Switches depend upon general memory allocation logic, Y1, Y7 and the Clock. Decode Y Switch 2, 4 is activated by two different conditions. In the memory operation section we stated that we would gate our drivers and switches to operate upon four even cores, upon four odd cores, and then we would step to the next byte to operate upon four more even cores and finally upon the last four odd cores.

Decode Y Switch 2, 4 is the circuit that will step us to the second byte when we operate upon a 16 core register. Bit Time Counter B is up during the last two bit times of each Instruction Time cycle. When Bit Time Counter B is true, the Decode Y Switch 2, 4 output will also be true. The other condition to turn on Decode Y Switch 2, 4 is Select Memory Upper with Y1. The only time this circuit is used is when we want to operate upon only 8 bits of data. If we have Select Memory Upper true with Y1, the Decode Y Switch 2, 4 would be true throughout all four bit times during an Instruction Time cycle. Therefore no change would take place to make us step to another Y switch. Decode Y Switch 3, 4 is active with all special addresses and is also active when the upper portion of memory is being addressed if Y 7 is true.

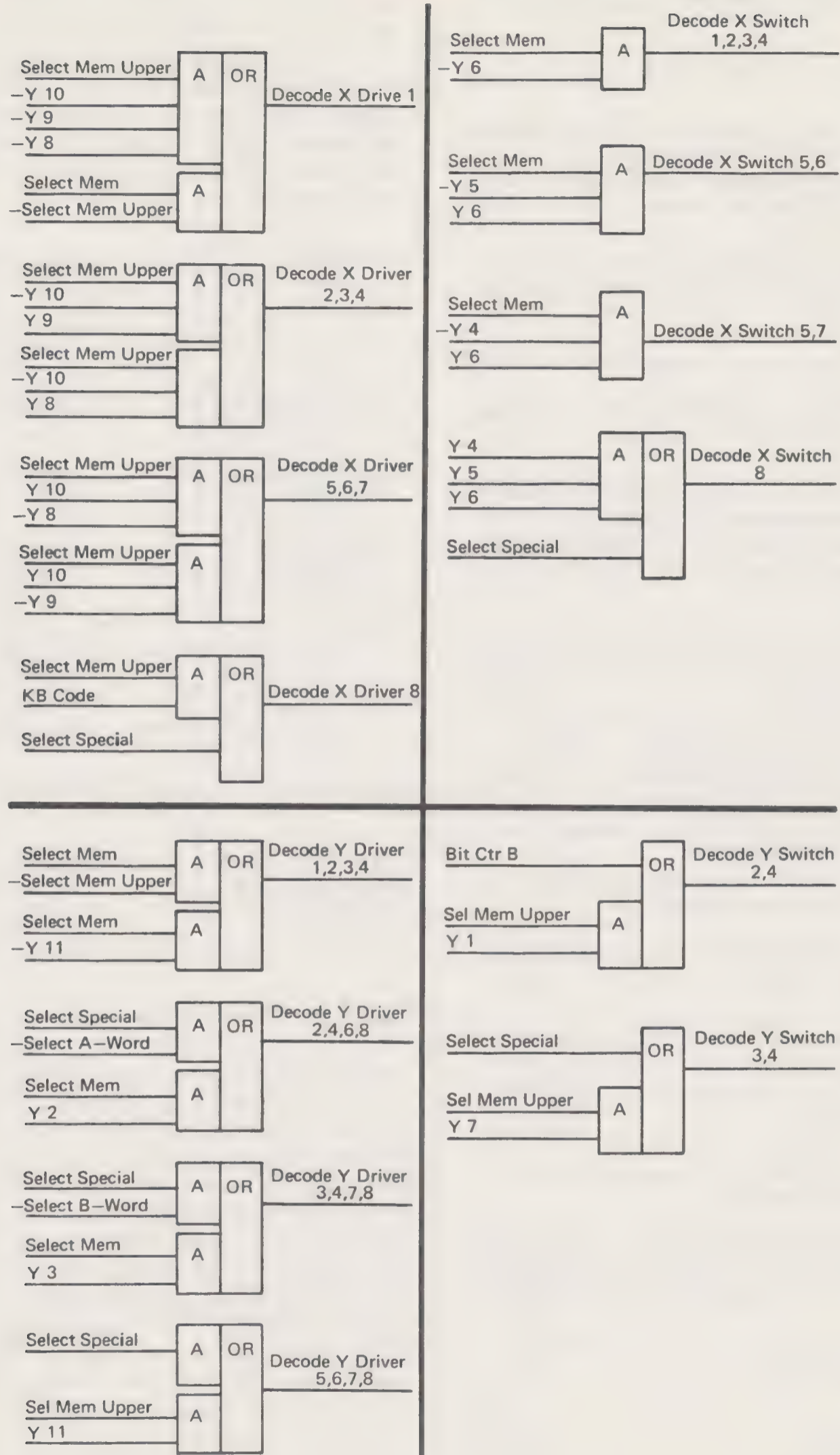


Figure 2 - Memory Decode Logic

## SUMMARY

The decode of the X Drivers is dependent upon the states of memory allocation logic combined with the outputs of Y8, Y9, and Y10.

1. When Select Special is true - Decode X Driver 8 is selected.
2. When Select Memory is true and Select Memory Upper is false - Decode X Driver 1 is selected.
3. When Select Memory and Select Memory Upper are both true Y8, Y9, and Y10 will be decoded.

The decode of the X Switches depends upon the states of Select Special and Select Memory combined with the combinations of Y4, Y5, and Y6.

1. When Select Special is true - Decode X Switch 8 is selected.
2. When Select Memory is true Y4, Y5, and Y6 will be decoded.

The decode of the Y Drivers is dependent upon the states of particular special address signals in addition to general memory allocation logic. The decode of the Y Drivers is also controlled by general memory allocation, combined with the outputs of Y2, Y3, and Y11.

1. When Select Program Step Address is true — Decode Y Dr. 2, 4, 6, 8 and Decode Y Dr. 3, 4, 7, 8 and Decode Y Dr. 5, 6, 7, 8 is selected.
2. When Select A-Word is true — Decode Y Dr. 3, 4, 7, 8 and Decode Y Dr. 5, 6, 7, 8 is selected.
3. When Select B-Word is true — Decode Y Dr. 2, 4, 6, 8 and Decode Y Dr. 5, 6, 7, 8 is selected.
4. When Select Memory is true and Select Memory Upper is false Y2 and Y3 will be decoded.
5. When Select Memory and Select Memory Upper are both true, Y2, Y3 and Y11 will be decoded.

The decode of the Y Switches depends upon the Clock and general memory allocation logic combined with Y1 and Y7.

1. When Select Special is true, Decode Y Sw. 3, 4 will be selected during Bit 1/4 time and Bit 5/8 time. Both Y Sw. 2, 4 and Y Sw. 3, 4 will be selected during Bit 9/12 time and Bit 13/16 time.
2. When Select Memory and Select Memory Upper are both true Y1 and Y7 will be decoded.

For our I—O cycle, the Select Special signal in our general memory allocation logic is up. The Select Program Step signal is also up. All other outputs in the memory allocation logic are down.

Select Special will select the following decodes:

Decode X Driver 8  
 Decode X Switch 8  
 Decode Y Driver 2, 4, 6, 8  
 Decode Y Driver 3, 4, 7, 8  
 Decode Y Driver 5, 6, 7, 8  
 Decode Y Sw 3, 4 during Bit 1/4 and Bit 5/8 times  
 Decode Y Sw 2, 4 and Decode Y Sw 3, 4 during  
 Bit 9/12 and Bit 13/16 times

## GATES

With these decodes in mind let's proceed to the actual switch and driver logic used to select the lines to memory. First we will examine the GATES to tie X Drivers and X Switches (Fig. 3). The And Gates shown on the left sides of the drivers and switches is composed of logical signals from the Memory Address decode circuitry combined with logical signals from the Memory Address Latches. The Gates are used to set up the selection of one X Driver and one X Switch for each address in memory.

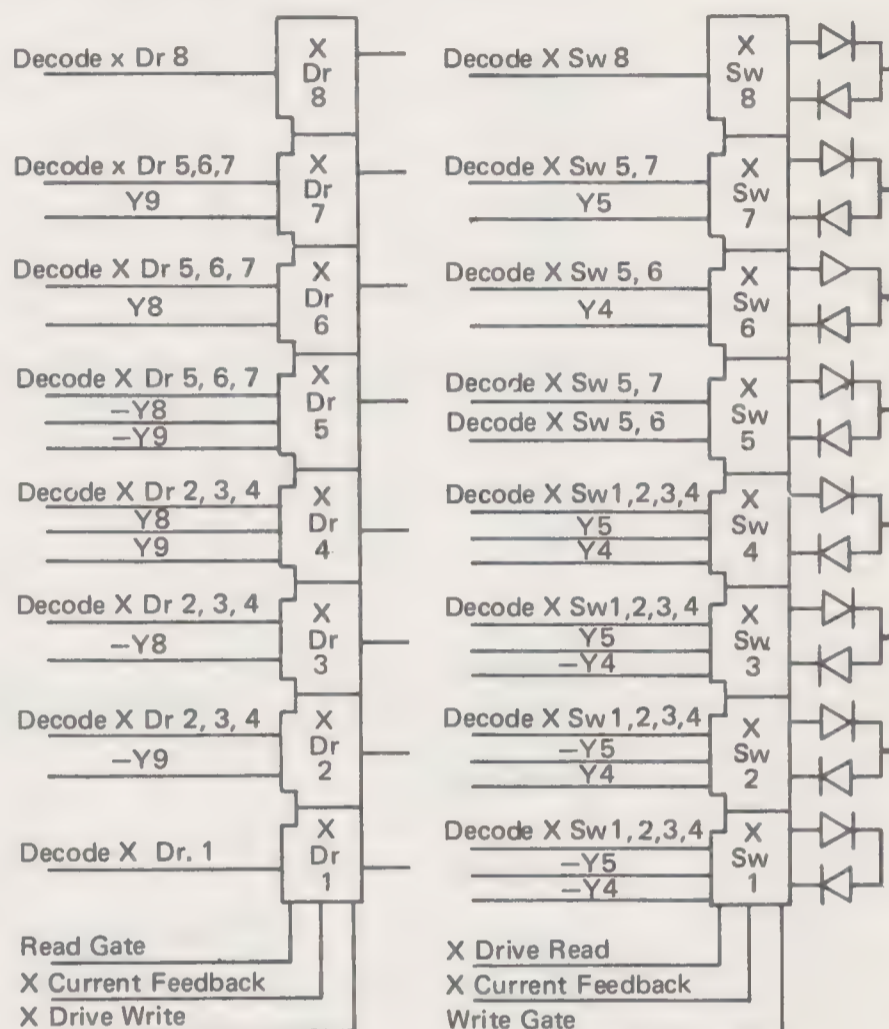


Figure 3 - X Driver And Switches

Before any of the drivers or switches can turn on, three other gates must be satisfied for each. In memory operation, you learned that current flows from the driver to the switch at read time and from the switch to the driver at write time. Gates are provided to direct the currents in the proper direction at the proper time. The READ GATE and X DRIVE READ signals are generated while Time Write clock signal is down. The WRITE GATE and X DRIVE WRITE signals are generated while Time Write signal is up. These read and write gates control the direction of current through the X lines. The final gate required to select an X driver/X switch combination is called X CURRENT FEEDBACK. The X Current Feedback signal is generated by the X half select current and lasts for one SSA or SSB time. The X Current Feedback signal becomes true for each memory operation.

The Y Driver and Y Switch gating logic is similar to the logic required to gate the X Drivers and Switches. The Y Drivers are gated by the Y Driver Decodes and Memory Address Latches in conjunction with current direction and current time signals (Fig. 4). The current direction gates (Read Even - Write Odd Gate, and Y Dr Read Even-Write Odd, Read Odd-Write Even Gate and Y Dr Read Odd-Write Even) are controlled by

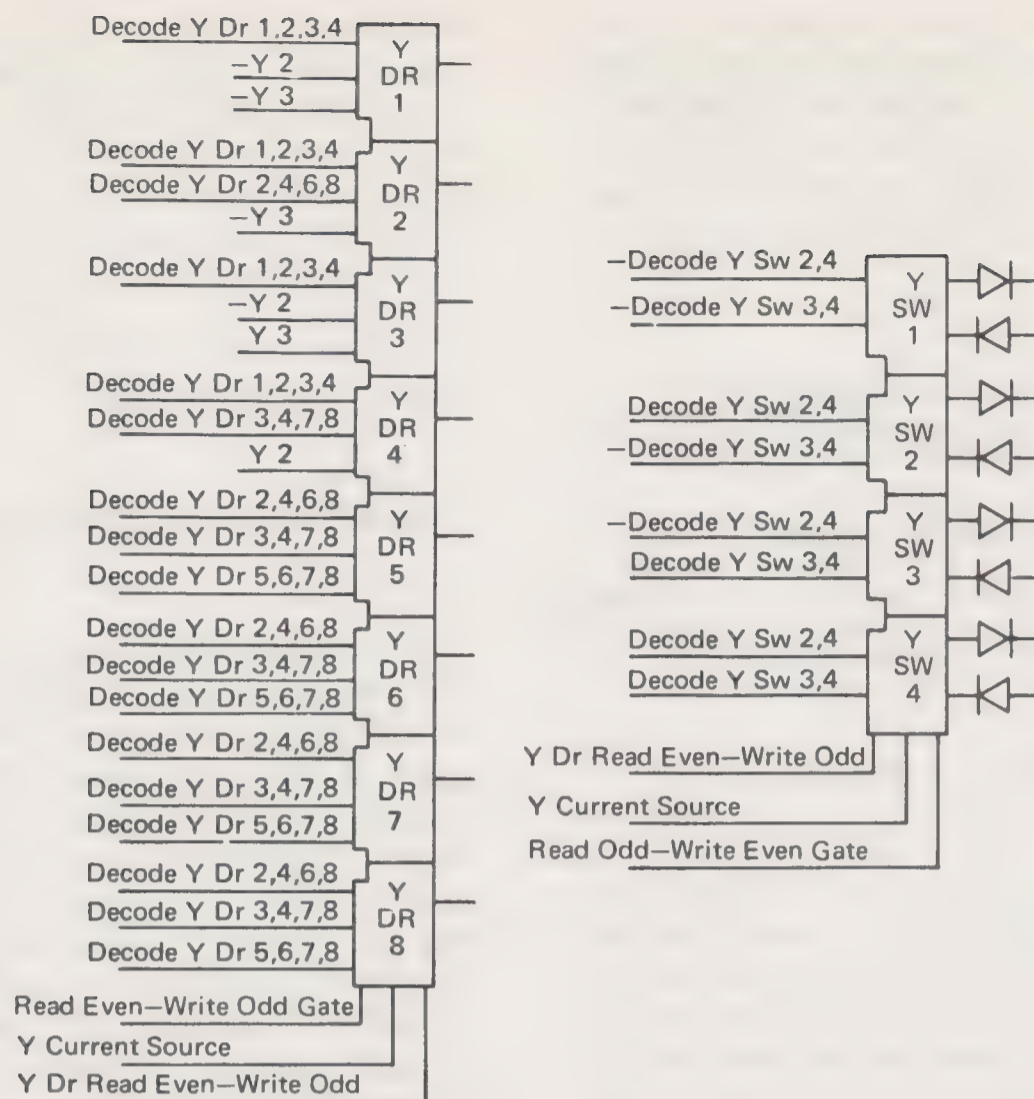


Figure 4 - Y Drivers And Switches

logic generated by the Clock. The Read Even - Write Odd gates are true during the first and third read times and during the second and fourth write times in each Instruction Time cycle. The Read Odd - Write Even gates are true during the first and third write cycles and during the second and fourth read cycles. (This gate timing allows us to read the even cores from two memory locations, write the even cores in those same locations, and then read the odd cores from the defined location and finally to write the odd cores in the same location (Fig. 5). In a P-Only cycle, the Read Q Time would not appear. The Memory Address Decode logic and Memory Address Latches have been selected to gate one Y Driver and one Y Switch at a time. The Read Even - Write Odd Gates or Read Odd - Write Even Gates will select the direction of current flow. Finally, the X and Y Current Sources will turn on the drivers and switches.

In Instruction Time 0 (Zero), the Clock has selected the Program Step Address Register to be operated upon. Select Program Step Address is up. Select Special is also up (Fig. 1). Due to these signals, Decode X Driver 8 and Decode X Switch 8 are up. Decode Y Driver 2, 4, 6, 8, Decode Y Driver 3, 4, 7, 8 and Decode Y Driver 5, 6, 7, 8 are up. Decode Y Switch 2, 4 will be down during the first two bit times but will be up during the last two bit times. Decode Y Switch 3, 4 will be up (Fig. 2). Decode X Driver 8 will select X Driver 8. Decode X Switch 8 will select X Switch 8 (Fig. 3). With Decode Y Dr 2, 4, 6, 8, Decode Y Dr 3, 4, 7, 8 and Decode Y Dr 5, 6, 7, 8 all up, Y Driver 8 will be selected. With Decode Y Sw 2, 4 down and Y Sw 3, 4 up during the first two bit times, Y Switch 3 will be selected. With one X Driver, one X Switch, one Y Driver and one Y Switch selected only the bottom gates are needed to turn on the current.

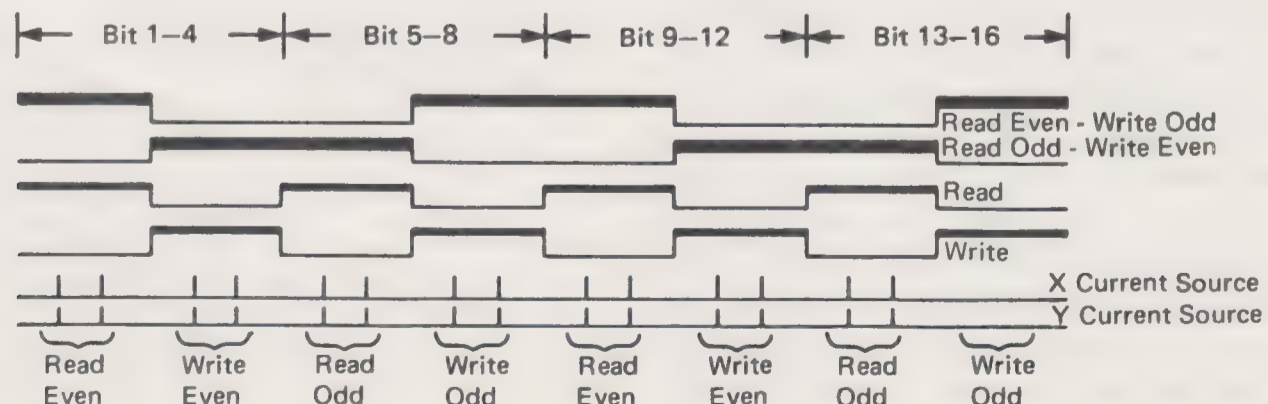


Figure 5 - Gates to Memory (P & Q Cycle)

The Read and the Read Even (Write Odd) gates will be satisfied during the first X and Y Current Source cycle (P-Read time). The first four cores in the Program Step Address Register will be operated upon. The cores will be read and any bits sensed will be amplified and passed on to the P-Buffer. There will be no second read cycle (Read Q-Time) during the I-O time (Fig. 6).

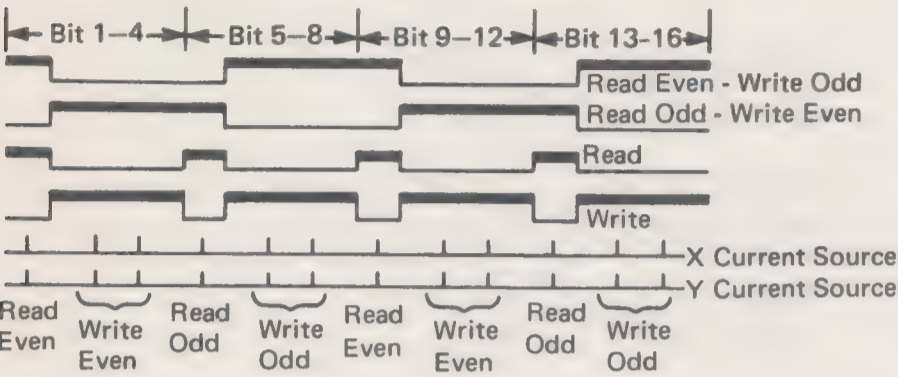


Figure 6 - Gates to Memory (P Only Cycle)

During the first write cycle, the EVEN INHIBIT lines will all be turned on to prevent writing at Q-Time. The write controls will be off during the I-O Write Q-Time. During the second write cycle (Write P-Time) the Inhibits will be under control of the Accumulator so that the proper bits will be written into the cores read at Read P-Time. During the next bit time, the Read signal and the Read Odd (Write Even) signal will be true. When the X and Y Current Sources become true at Read P-Time, the second group of 4 bits are read from the Program Step Address Register, sensed and passed on to the P-Buffer.

All ODD INHIBITS are activated at Write Q-Time, thereby inhibiting writing data into the cores. At Write P-Time, the odd cores are written with the Inhibits under Accumulator control. During the third bit time, Bit 9/12 time, the Decode Y Switch 2, 4 becomes true and Y Switch 4 is selected and Y Switch 3 is de-selected. At Read P-Time the four even cores on the wire from Y Driver 8 to Y Switch 4 are read and written. Finally the four odd cores in the X-Y current paths are read and written.

During I-O time the quantity "two" was added using the accumulator so that the Program Step Address Register would be updated to the address of the next step to be done. Two was added because each program step is two bytes (one register) in length. All addresses to memory are numbered in bytes.

As you have seen the memory allocation logic gives the machine the ability to select special addresses (words) in memory or select locations defined by the Memory Address Latches. All or part of the Memory Address Latches are decoded depending upon the state of the Select Memory Upper signal. There are 11 Memory Address Latches, Y1 through Y11. If Select Memory is true while Select Memory Upper is false, Y2 through Y6 will be decoded ignoring the state of the Y1 Latch and Y7 through Y11 Latches. In order to decode all 11 Y Latches, Select Memory Upper must be true. This memory allocation logic gives us the ability to use the Y1 and Y7 through Y11 Latches for purposes other than addressing memory. These purposes will be covered later.

The Memory Address Latches are arranged so that the address number is the binary equivalent of the Memory Address Latches (Fig. 7). For example: If Y8 Latch were set and all other latches were reset, Register 128 would be addressed when Select Memory and Select Memory Upper were both true. If only Select Memory were true in the memory allocation logic, Register 0 would be addressed.

Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
1024	512	256	128	64	32	16	8	4	2	1

Figure 7 - Binary Arrangement of Memory Address Latches

The Memory Address Latches are first loaded at I-O time while the data from the Program Step Address Reg. was in the P-Buffer. A signal named LOAD Y is generated by Clock signals at I-0, I-2, I-4 and I-8 times. The Load Y signal is anded with the information in the P-Buffer to set the appropriate Y Latches. As stated in Machine Organization, this is essentially a transfer of data from the Program Step Address Register in memory to the Memory Address Latches. Let's forget about even and odd locations in memory and arrange the data in the order that it is read from memory (Fig. 8). Bit 1/4 will be read and written first. Bit 5/8 will be operated on second, Bit 9/12 third, and finally Bit 13/16 will be read and written. If the machine had just been turned on and reset, the bit configuration shown in Fig. 8 would be in the Program Step Address portion of memory.

BIT NO.															
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	0	0	0	0	0	1	0	0	0	1	0	0	0	1	0

Figure 8

At Read-P Time the first four bits of data would be read and latched into the P-Buffer. While the data is in the P-Buffer, the Load Y signal generated by the Clock would be anded with the P-Buffer and with the Clock signal Bit 1/4. Y2 would be set (Fig. 9). All other Y Latches would remain off because their inputs are not satisfied at this time. A "2" would have been added at this point and the accumulated total would have been written back into the cores that were read at P-Time. The P-Time Buffer would then be reset for the next bit time.

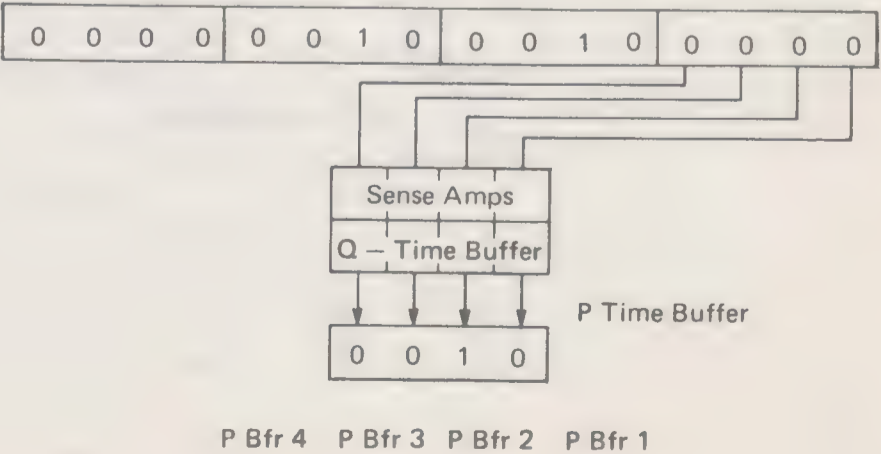
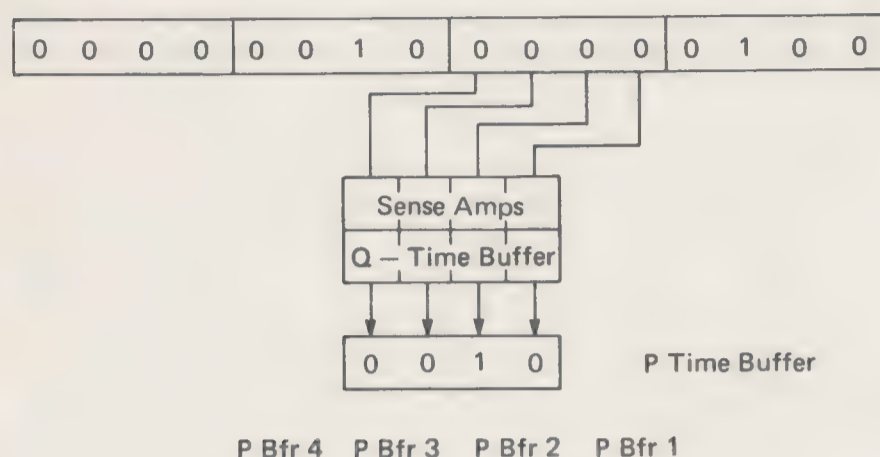


Figure 9

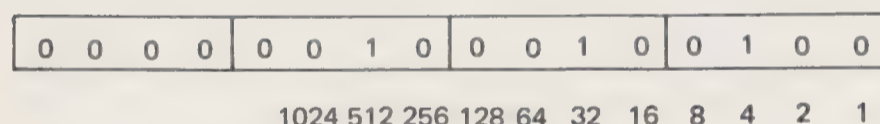
Timing diagram for the P Time Buffer. The input vector is 0 0 0 0 0 0 1 0 0 0 0 0 0 1 0 0. The Sense Amps output to the Q-Time Buffer, which then outputs to the P Time Buffer. The P Time Buffer output is 0 0 1 0.

P Bfr 4   P Bfr 3   P Bfr 2   P Bfr 1



Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	1	0	0	0	1	0	0	0	1	0
1024	512	256	128	64	32	16	8	4	2	1
Binary									1 = Set 0 = Reset	

The program step address written back into memory appears as shown in Fig. 12. At the conclusion of I—O time, the Memory Address Latches contain the address 546 that was previously in the Program Step Address Register. The Program Step Address Register now contains the address 548.



During the next instruction time, Instruction 1 Time, the memory allocation logic will decode all of the Memory Address Latches during P-Time. The switches and drivers will be gated to address the program step that is contained in Bytes 546 and 547. During Q-Time, the switches and drivers will be gated to address the A-Word in the special area of memory. The program step read from memory will be written into the A-Word and will also be written back into the memory location 546.

To set the Y Latches, a complete Instruction Time cycle is required. To utilize the outputs from the Y Latches, another Instruction Time cycle is required.

Some program steps, such as Indirect Arithmetic operations, require as many as four different memory locations to be addressed just to perform the step. The Memory Address Latches are loaded during Instruction Times 0, 2, 4, 6 and 8. They are reset during those same "I" Times just prior to being set. The loading of the Y Latches is unique at I—6 Time and during I—2 Time in an Incremental Jump. The special loading conditions will be discussed in program step operation.



## CCU OPERATION

### Q-BUFFER

The Q-Buffer consists of 4 triggers which are a part of the sense amplifier circuitry. As data is read from memory four bits at a time, it is stored in the Q-Buffer. During Read P Time the Q-Buffers will set the corresponding P-Buffers. The Q-Buffers will then be reset prior to Read Q Time. Data read at Read Q Time will not affect the P-Buffers but will remain in the Q-Buffers. Since the Accumulator is fed by outputs of both the P-Buffer and Q-Buffer a sum or difference will now be available in the Accumulator.

Q-Buffer 1 and Q-Buffer 2 may also be set during Bit 1/4 Time so we may "bump by 1" during an indirect cycle or "bump by 2" during a normal cycle.

### P-BUFFER

The P-Buffer is used to store 4 bits of data acquired, either from memory or from an input device, until it is processed.

The P-Buffer is composed of 4 latches. The latches are set during Read P-Time for internal CCU operations. At Read P-Time read currents flow through memory. The cores that contain "ones" will be flipped and induce A.C. signals in the sense lines. These signals are amplified by the Sense Amplifiers. The Sense Amplifier outputs set the Q-Buffers. The Q-Buffer outputs will then set their respective P-Buffer Latches. The data stored in the P-Buffer will remain there throughout one bit time. At the completion of each bit time the P-Buffer is reset so the next group of 4 bits can be processed.

Other conditions to set the P-Buffer Latches are controlled by the I/O Control logic. An INPUT STROBE signal becomes true at the proper Instruction Time so that data from the INPUT DATA LATCHES can be transferred to the CCU. The Input Strobe signal is anded with outputs from the Input Data Latches to set the proper P-Buffer Latches. Another signal developed by the I/O control logic is KEYBOARD ENTRY STROBE. The Keyboard Entry Strobe signal is anded with outputs from keyboard decode circuitry so that bits can be transferred from the keyboard into the CCU's memory.

The outputs of the P-Buffers are used to set the Memory Address Latches, set the Operational Code Latches, set the Output Latches and to control the inhibit logic into memory if the write controls define "Write from P-Buffer".

The outputs of the P-Buffers are also directly connected to the accumulator.

### ACCUMULATOR

The Accumulator consists of four accumulator circuits, four carry circuits, plus a carry-over latch. Outputs from the P-Buffer (data read at Read P-Time) are anded with outputs from the sense amp triggers (data read at Read Q-Time) to give a total or sum output from the Accumulator. The Accumulator output is dependent upon signals named Add or Not Add (subtract) for the actual output signal level.

Let's use an example to demonstrate the operation of the Accumulator. Let's add 43 to 25.

Since a core in memory has only two states, "1" or "0", Binary Arithmetic is used for calculations. The simple rules for binary addition are:

$$\begin{aligned} 0 + 0 &= 0 \\ 0 + 1 &= 1 \\ 1 + 1 &= 0 \text{ with 1 Carry} \end{aligned}$$

Our example will appear in memory as follows:

	128	64	32	16	8	4	2	1	
43 =	0	0	1	0	1	0	1	1	P-Buffer
25 =	0	0	0	1	1	0	0	1	Q-Buffer
68 =	0	1	0	0	0	1	0	0	Accumulator

Let's assume that the 43 is located in the memory location that is read at P-Time and that the 25 is located in the memory location that is read at Q-Time. At Read P, Bit 1/4 Time, the first four bits of the quantity 43 is read and latched into the P-Buffer. At Read Q, Bit 1/4 Time, the first four bits of the quantity 25 are read from memory and left in the Q-Buffer.

The P-Buffer is in the following state: 1011

The Q-Buffer is in the following state: 1001

The CARRY OVER LATCH output is false because it was reset at the very beginning of the Instruction Time cycle now in progress. Since the Carry Over latch output is down and both P-Buffer 1 and Q-Buffer 1 are true, the Accumulator 1 circuit will not become true. However, the Carry 1 circuit will be true  $1 + 1 = 0$  with 1 to carry in binary arithmetic.

The Carry 1 output (up) is anded with the P-Buffer 2 output (up) and with the Q-Buffer 2 (down) and the Accumulator 2 output remains down. Carry 2 will be turned on.  $1 + 1 + 0 = 0$  with 1 to carry.

The Carry 2 output (up) is anded with the P-Buffer 3 output (down) and with the Q-Buffer 3 output (down). Accumulator 3 is turned on. With these outputs the Carry 3 circuit remains off.  $1 + 0 + 0 = 1$  with no carry.

With the Carry 3 output down and the outputs from P-Buffer 4 and Q-Buffer 4 both up the Accumulator 4 output will not come on. The Carry 4 circuit will come on.  $0 + 1 + 1 = 0$  with 1 to carry.

The up level output from Carry 4 will set the Carry Over Latch which will be anded with the outputs from P-Buffer 1 and Q-Buffer 1 in the next bit time. In order to accumulate all data from each of two different memory locations, the same accumulation sequence is followed for the 4 bit times.

If a subtract operation is required the NOT ADD signal is being generated by the operational code decode circuit and the Accumulator outputs will result in subtracting the Q-Buffer from the P-Buffer.

The Accumulator is used to perform its arithmetic function in only the last Instruction Time (I-9 Time). It is used at other times as well, but at these times either the P-Buffer or the Q-Buffer will contain all zeros except for Bump by 1 or 2. With zeros in one of these two circuits only the contents of the one containing data will appear at the output of the Accumulator circuit.

The Accumulator outputs are used to control the Inhibit lines when the Write Accumulator signal is true.

## OPERATIONAL CODE LATCHES

Seven operational code latches are used to define the operation that the processor is to perform during any program step. The operational code is contained in each program step in memory. In I-0 time the address of the program step to be done was loaded in the memory address latches (Y latches). In I-1 time this address is used to read out the program step. The memory allocation logic will decode all 11 Y latches at P-Time. At Read P-Time the bits from the program step will be latched in the P-Buffer. While the bits are in the P-Buffer, Clock signals will generate a LOAD OPERATIONAL CODE LATCH Signal. The Load Operational Code Latch output is anded with the data in the P-Buffer to set the Operational Code Latches.

The Operational Code Latches are loaded only at I-1 Time. The latches will remain set throughout the program step being performed.

The operational code set into the latches is decoded to define the type step in progress. Six circuits are used to decode the OP Code Latches. The outputs of the decodes are called:

1. Arithmetic Operation
2. Jump
3. Immediate

4. Program Control
5. Incremental Jump
6. Input/Output

The outputs of the decode circuits are used in conjunction with the outputs of the Operational Code Latches to control the Clock, control some memory addresses and to control add and subtract functions of the Accumulator.

## LOW AND EQUAL LATCHES

The Low and Equal latches give the CCU the ability to react to the results of its calculations.

The Equal Latch is set and the Low Latch is reset at I-8 Time just prior to the I-9 cycle when an arithmetic calculation is made.

At I-9 Time the output signals from the Accumulator and a decode called ACCUMULATOR NOT=ZERO are used to change the states of the Low and Equal latches depending upon the results attained.

If a positive Accumulator output resulted the Equal Latch would reset because the Accumulator Not=Zero would be true.

If a zero result were attained (Example: Compare quan. 2 to quan. 2) neither latch would change state. An equal condition is defined by Not Low (high) and Equal.

If the result from a calculation were negative both latches would change state (Example: Compare 4 to 2). The Low Latch would set. When the Low Latch sets the Equal Latch resets.

The Low and Equal latches will remain set until the next I-2 Time comes along. If several types of conditional jump steps follow, the Low and Equal latches will remain set because branch operations use only I-0 and I-1 Times if the jump conditions are not satisfied.

The Low Latch can also be set by a signal developed from the Tape Reader called SET LOW. This signal is generated when the skip button has been depressed on the Tape Reader. A Jump on Low step follows an Input Instruction so that a space can be installed in the output copy by the program if a parity error occurred.

The outputs from the Low and Equal latches are anded with outputs from the Operational Codes when a conditional jump step is being performed. If the conditions of the latches match the conditions defined by the Operational Code a signal called TAKEN is generated at the end of I-1 Time. If Taken is true at the end of I-1 Time during the jump step the Clock will permute to I-9 Time to transfer the new address of the next step to the Program Step Address Register. If Taken is false at the end of I-1 Time the Clock will permute back to I-0 time and perform the next step in the program.

## WRITE CONTROLS

The Write Controls are made up of two circuits that are used to gate the Current Sources. The circuit outputs are named WRITE P-BUFFER and WRITE ACCUMULATOR. The Write Controls are gated by the Clock. In some cases, Operational Codes are anded with Clock signals to prevent writing during certain operations. Clock signals alone prevent writing during particular Instruction Times.

During most Instruction Times we write from the P-Buffer at Write Q-Time and write from the Accumulator at Write P-Time. We never write from the Accumulator at Write Q-Time but in some cases we do write from the P-Buffer at Write P-Time.

## CURRENT SOURCES

Four Current Source signals are used to control the logic to the Inhibit lines. The CURRENT SOURCES are controlled by the outputs from either the P-Buffer or the Accumulator depending upon Write Control signals.

Since Inhibit currents are used to leave cores in zero states, the Current Source outputs must remain true to prevent writing the cores. For instance, if the P-Buffer 1 contained a "one" (up level) and the Write from P-Buffer signals were true the Current Source 1 signal would go to a down level. The 1 bit position would be written into memory at Write Time.

The Current Sources are also controlled by a signal named Edit Program Control Bit during a program control program step.

## I/O CONTROL

I/O Control logic is used to direct data into or out of the CCU. It is also used in conjunction with the Y8, Y9, and Y10 Memory Address Latches to choose the proper device for Input/Output Program Steps. The outputs from the I/O Controls generate signals to strobe the Reader Data Latches, Console Keybuttons, and Loading of the Output Register. The controls also define the times when the Output Register will send its data to either the Translator or Lights.

Twelve circuits are used to control the Input/Output Data Flow. The actual input or output of data occurs during I-5 Time of the step. If the device selected is ready, the data will flow either to or from the CCU. If the device is not ready, the CCU must not go on to the next program step, but must wait until the selected device is ready. To prevent the CCU from bypassing an Input/Output step a circuit called INHIBIT is turned on. The Inhibit circuit makes the CCU repeat the Input/Output step until the device is ready. When the device finally becomes ready the Input/Output step is performed and the program continues.

In order to turn the Inhibit circuit on and off at the proper time, a PRE-INHIBIT LATCH is used. The output of the Pre-Inhibit latch is anded with the -Bit Time Counter A signal so that Inhibit will occur at the beginning of an Instruction Time.

The Pre-Inhibit latch is operated by several different condi-

tions. If an input from the Tape Reader operation is in progress the Pre-Inhibit latch will turn on in I-2, Bit 13/16, Write Time while pulse B is false if the Tape Reader has not yet developed a CHARACTER READY SIGNAL. If the Tape Reader has a character ready the Pre-Inhibit latch will not come on. If Pre-Inhibit were on because the Tape Reader did not have a character ready the Inhibit Latch would be set at the beginning of I-5 Time.

The Pre-Inhibit latch is also set while a keybutton on the console is held down during a keyboard input step. The inhibit function prevents the program from continuing, thereby allowing only a single entry per cycle.

The Pre-Inhibit latch will set during output steps to the Translator if the Translator is not ready or if a multiplex operation is in progress. However, if we are outputting to the lights, they are considered as always being ready.

The C.E. Edit switch also sets the Pre-Inhibit latch to prevent the program from running while the C.E. is examining various addresses or data.

The Pre-Inhibit latch is reset by an UPSET PRE-INHIBIT signal anded with the Begin Write Time Clock signal. Upset Pre-Inhibit occurs during I-1, Bit 13/16, Time Write when the B Clock signal is down. After being reset the Pre-Inhibit latch will immediately set again if the I/O devices are not yet ready.

The Inhibit Latch output prevents the program from proceeding by preventing the "2" from being added to the program step address during the next I-0 Time.

The Input or Output step in progress must continually be attempted until the device is ready. Since the Select Program Step Address Reg. was updated prior to finding out what type step was to be done we must shift our memory address control so that the Input/Output program step will be addressed. During the I-1 cycle when we read the Input/Output program step from memory we wrote the step into the A-Word portion of memory and also rewrote it in the memory location from which it came. If Inhibit is true the memory allocation logic will only address the A-Word during succeeding I-1 Times. The A-Word data is identical to the I/O program step. During each I-1 cycle the A-Word will be read and rewritten and the Operational Code Latches will be set from the A-Word data. When the device is ready, Pre-Inhibit and Inhibit will go off and normal memory address cycles will occur.

As previously stated all Input/Output data is transferred at I-5 Time. The Output Latches are also loaded at I-5 Time. The Load Output Latch signal occurs during any Output step at I-5 Time if the output device is ready. If the Translator is not ready we do not reload the Output Latches because the Translator magnets must be held until we are well into its mechanical cycle. A BUSY LATCH is used for this purpose. The Busy Latch output prevents reloading the Output Latches and resetting a circuit whose output is named READY. The Ready Signal is anded with Output Instruction and Clock signals to direct data to the proper output device by a circuit called SELECT OUTPUT DEVICE. The device is selected in I-2 Time even though it will not be activated until I-5 Time.

Data can be inputted from either the Input Data Latches or from the console keyboard. In order to transfer data at the proper time from the proper device two circuits are used. If the program step is an input from the Tape Reader an INPUT STROBE signal will occur at I-5 Time during the time that Central Bit Time is up, if Inhibit is down. The Input Strobe signal is anded with the outputs from the Input Data Latches to set the P-Buffer latches at the proper time. If a Keyboard input program step is in progress a Keyboard Strobe signal occurs at I-5 Time when Central Bit Time is true. The Keyboard Strobe signal also is true at I-0 Time if the CE Edit Switch is in address or at I-1 Time if the CE Edit Switch is in the data position. If the switch is in any position other than process the Edit latch will come on. A latch is used to control the Edit mode so that a program step will not be interrupted when the C.E. changes the switch position.

The CCU has the ability to output data in a multiplex mode of operation. An output multiplex program step causes the CCU to output a line of type one character at a time to the Translator whenever it is ready to accept it. One output multiplex program step is all that is needed to output the entire line. The program continues to operate in the multiplex mode except when the Translator is ready to accept another character. When the Translator is ready, the normal program sequence is interrupted and an Output step occurs. The last character in each line of processed characters is a HALT CODE. The Halt Code consists of "1's" in all 8 bit positions of the byte containing this character. When the Output Register is loaded with the Halt Code a signal called HALT is developed. The Halt signal

resets the Multiplex Latch and the CCU reverts back to its original control.

With Multiplex "on" the program will operate in a normal manner until Ready comes true. When Ready comes true the CCU continues through I-0 and I-1 Times in the normal manner except the Load Operation Latch signal does not occur. The program step being addressed at I-1 Time was read and written into the A-Word and rewritten back into its memory location but the Operational Code Latches were not loaded as usual. Near the end of I-1 Time after Write P-Time the Upset Pre-Inhibit signal comes true. The Upset Pre-Inhibit signal is anded with the output from the Multiplex Latch and the Ready signal to set the Operational Code 4 latch and the Operational Code 6 latch. Operational Codes 4 and 6 define an Output step. Multiplex is then anded with the Operational Code decode circuit named Output to turn on the Pre-Inhibit Latch. We have effectively forced the CCU into an Output step and have turned on the Inhibit Latch. The output device is ready and the output step is performed.

At the beginning of this cycle the interrupted program step had been written into the A-Word. Since Inhibit is on the A-Word will be addressed at the next I-1 Time. During this next I-1 Time the Translator is no longer ready so the Operational Code Latches will be loaded. Since the A-Word is being addressed and the Load Operational Code Latch signal is true, the Operational Code Latches will be loaded with the program step that was interrupted. Of course the inhibit function prevented adding "2" to the Program Step Address Word.

## PROGRAM STEP OPERATION

### INTRODUCTION

In the following discussion of the Program Step Operation it will be assumed that you have a good understanding of the Memory Address logic used in the CCU. If not, it would be a good idea to review the section on Memory Address before proceeding.

Each program step performed by the Composer Control Unit is accomplished by controlling the Memory addresses and Write Controls in respect to Clock times. The program step will dictate which Instruction Times must be used.

The CCU is basically a one address machine. During a given "I" Time (Read-Write cycle) we may address two different Memory locations. Remember, however, that the General Memory address must be controlled by the Memory Address Latches while the other address (Special Registers) is controlled by the Clock. We cannot address two General Memory addresses during the same "I" Time. Two Special Registers may be addressed during the same "I" Time, however, because their addresses are controlled by the Clock.

During some "I" Times it is not necessary to address two different locations in Memory. In these cases the Clock circuits will generate a P-ONLY CYCLE and only one Memory location will be read and written. As the name implies, this will be done during Read P Time and Write P Time. There will be no Read Q Time developed by the Clock although Write Q Time will be.

When we examine the Instruction Time Flow Chart, it becomes evident that all ten "I" Times are not always necessary to perform the operations called for by the program. A minimum of two "I" Times is used during Branch (Jump) not Taken, while a maximum of ten "I" Times is used during P and Q Indirect Arithmetic. Each of the ten "I" Times is unique and permuting of the "I" Time Counter allows any sequence combination necessary to perform the program step.

Each Instruction Time will be discussed in detail. However, since I-0 and I-1 are practically identical for all operations, they will be discussed first.

#### I-0 TIME (P ONLY CYCLE)

The purpose of I-0 Time is to locate the program step to be performed. Since the CCU is a stored program machine, the program step will already be in one of the 16 bit Registers in the program area of Memory. The Program Step Address Register contains this Memory address. We need to read this address from the PSAR, set the Memory Address Latches, add "2" to the original data and rewrite this updated data back into the PSAR. Since program steps are normally located in

successive Registers, the PSAR is "bumped" by 2 so it will contain the address of the next step.

During Read P, Bit 1/4 Time the Clock will condition the address of the PSAR. The first four bits of data are read, sensed by the Sense Amps and set in the P-Buffer. When Central Bit Time comes true, a signal called Load Y will come true. Load Y is anded with the outputs of the P-Buffer and sets the corresponding Memory Address Latches (Y's). The first four bits of the PSAR step have been transferred to their corresponding Y latches.

The Sense Amp Triggers (Q-Buffer) are reset and since there is no Read Q Time they will receive no data from Memory. However Q-Buffer 2 will be set by I-0, Bit 1/4, Bump Strobe Time. The Accumulator now contains the data read at Read P Time plus the "2" just added from the Q-Buffer.

Neither Write Control will be satisfied at Write Q Time. We will be addressing the PSAR but no change can occur with the Write Controls down.

At Write P Time the Write from Accumulator signal is satisfied and comes true. The data in the Accumulator (Original first four bits plus the 2) will be written into the PSAR. We are now at the end of Bit 1/4 Time and have read the first four bits, loaded the first four Y's, added 2 and written the updated data back into the first four bits of the PSAR.

Bit 5/8 and Bit 9/12 Times are identical except Q-Buffer 2 will not be set during these times. The data read from the PSAR is loaded into the corresponding Y's and then written back into the PSAR. Since there are only 11 Memory Address Latches and we have now read 12 bits, they are all loaded according to the bit data of the program step. The 12th bit is inhibited by holding Q-Buffer 4 reset during I-0, Bit 9/12, -B-TW

At the beginning of I-0, Bit 13/16 Time INHIBIT READ comes true. The -IR leg of the Q-Buffer goes false and prevents any bits read during Bit 13/16 Time being set in the Q-Buffer or P-Buffer. As previously mentioned, this would be invalid data anyway since we have no Y Latches left to load. Bits 13 through 16 of the PSAR must be kept clear to prevent the Low-Equal latches from being affected by arithmetic operations involving the PSAR.

All I-0 Times are the same with the exception that the "Bump by 2" will not occur during Edit mode or during Input/Output mode if the CCU must wait until another device is ready. This will be fully explained in the sections dealing with Edit and Input/Output modes.

At the end of I-0, Bit 13/16 Time the permute circuit will step the Clock to I-1 Time.

## I-1 TIME (P & Q CYCLE)

The purpose of I-1 Time is to read the program step in the Register addressed by the Memory Address Latches (loaded at I-0), set the Operational Code Latches, write this program step data in the A-Word and also write the unchanged data back into its regular Memory location. This is done so the program step data is preserved for future use. With the program step now duplicated in the A-Word we can use this A-Word data to perform the requirements of the step without fear of destroying or altering the program stored in the machine.

At Read P, Bit 1/4 Time, we address the program step under control of the Y Latches. The first four bits are read and set in the P-Buffer. While this data is in the P-Buffer, the LOAD OPERATIONAL CODE LATCH signal comes true at Central Bit Time. The Operational Codes are set to define the Program Instruction to be performed.

During Read Q Time of this cycle the address switches to the A-Word. INHIBIT READ comes true. This prevents any data that may have been in the A-Word from reaching the Q-Buffer. We have now cleared the first four bits of the A-Word.

At Write Q Time we are still addressing the A-Word. The Write from P-Buffer signal comes true and we write the first four bits of the program step into the A-Word.

As the Clock progresses to Write P Time, the address is again controlled by the MAL and we address the original program step location. The Write from the Accumulator signal comes true and the first four bits of the program step are written back into their original cores. It is permissible to write from both the P-Buffer and the Accumulator because we did not set any data in the Q-Buffer at Read Q Time. Therefore, the accumulation of data is P-Buffer plus zero or P-Buffer. In this case, the P-Buffer and the accumulator contain the same data.

Bits 5/8, 9/12, and 13/16 are identical except that different Operational Code latches will be loaded to correspond to the bits read.

At the end of I-1 Time the Operational Code Latches have been loaded, the program step has been written into the A-Word and preserved back in Memory. The next "I" Time will be under control of the Operational Codes. The Clock will be permuted under this control to the proper "I" Times necessary to perform the program operation defined by the Operational Code.

A small variation in the I-1 Time will occur if INHIBIT is true during Edit or Input/Output modes. This will be fully explained under the appropriate sections.

Before proceeding into a discussion of the individual Program Step Set operations, let's review what occurs during I-0 and I-1 Time.

During I-0 Time a P-Only cycle is performed. Clock control

will cause an address of the PSAR which contains the memory location of the next program step to be performed. This data is read and transferred to the corresponding Memory Address Latches. The data is increased by "2" and written back into the PSAR. We have updated the PSAR to locate the next sequential program step.

During I-1 Time a P&Q Cycle is performed. The Memory Address at P Time is under control of the MAL and we address the Program Step in Memory. At Q Time the address is controlled by the Clock and the A-Word is addressed. Inhibit Read is true during the Read portion of Q Time to clear the A-Word of any previous data. During Write Q Time the program step is written into the A-Word. Then at Write P Time the data is rewritten into the original memory location to preserve it for future use. Also, while the data was in the P-Buffer the Operational Code latches were loaded to identify the program step to be performed.

With the program data duplicated in the A-Word and the Operational Code latches defining the type of program step, we can now permute the Clock to the proper "I" Times necessary to complete the operation.

The various Program Step Sets will now be discussed individually. In each instance it will be assumed that the I-0 and I-1 Times have been performed and only the remaining "I" Times pertaining to the Program Step Set will be covered. All I-0 and I-1 Times should be considered identical to the previous paragraphs unless specific alterations are mentioned. It will be helpful to follow the Instruction Time Chart and the CCU function pages in the Reference Section.

## JUMP

The program step format for Jump will contain the number of the next program step to be performed. If the jump conditions have been met, a signal called TAKEN will be true and the Clock will permute from I-1 to I-9 Time. Since each program step is located by an address stored in the PSAR, the address data now in the A-Word must be transferred to the PSAR. Only one "I" Time (I-9) is needed to perform this transfer.

## I-9 TIME (P&Q CYCLE)

During Read P, Bit 1/4 Time our address circuitry is under control of the Clock and we will address the PSAR. However, Inhibit Read will be up during P Time of I-9 when Jump is up so no data will reach the P-Buffer during Read P Time.

At Read Q Time the address is again under Clock control and we will address the A-Word. The first four bits of the A-Word are read and stored in the Q-Buffers. Our Accumulator now contains A-Word data only since no data reached the P-Buffer during Read P Time, due to Inhibit Read being up.

At Write Q Time we are still addressing the A-Word, but neither Write Control is up. The first four bits of the A-Word are not written and remain clear from being read at Read Q Time.

The Write Accumulator signal is up at Write P Time and our

address is again switched to the PSAR. The first four cores are written from the Accumulator and we have transferred the first four bits of data in the A-Word to the first four bits of the PSAR.

Bit 5/8 Time is identical to Bit 1/4 except we will have read odd and write odd currents and operate on the second four bits of each address. The first 8 bits of data have now been transferred from the A-Word to the PSAR.

Bit 9/12 Time is identical to Bit 1/4 except Bit Time Counter B will be up and another Y switch will be selected and cause us to address the next four bits of each register (PSAR and A Word). Again we will be reading and writing even bits and the read and write even currents will be active.

Bit 13/16 Time is identical to Bit 5/8 except Bit Time Counter B is still up and we will read and write the last four bits using read and write odd currents. All sixteen bits of A-Word data have been transferred to the PSAR and the A-Word is now clear. Remember, however, that during the next I-0 Time when we read the PSAR and load the Y's, there will be no Y's to correspond to Bits 12 through 16. At the end of I-0 Time the top 5 bits of the PSAR will be clear because Inhibit Read will be up during Bit 13/16 Time of I-0. Also Bit 12 is killed by holding Q-Buffer 4 reset during Bit 9/12 of I-0 Time.

At the end of I-9 Bit 13/16 Time the Clock will permute to I-0 Time and the next cycle begins.

### JUMP (WITH LINK)

If a Jump with Link operation is to be performed, Operational Code 5 would have been set during I-1 Time. This is the basic difference between a normal Jump and a Jump with Link. Operational Code 5 will prevent the Clock permute to I-9 and will cause the Clock to step to I-2, I-3, and then to I-9. During I-2 and I-3 Times we will install our Link back to the main program routine in the first register of our sub-routine. At I-9 Time we will update the PSAR to take us to the second step of our sub-routine.

### I-2 TIME (P ONLY CYCLE)

During I-2 Time we will load the MAL with the address of the first register of our sub-routine. This data is contained in the A-Word format. The A-Word is transferred to the MAL, two is added to the A-Word data, and it is written back into the A-Word. The MAL will then contain our Link address and the A-Word will contain the address of the next register of our sub-routine, i.e., Link address plus 2.

During Read P, Bit 1/4 Time our address is under Clock control. We will read the first four bits, store this data in the P Buffer, and load the corresponding Memory Address Latches (Load Y will be up at Central Bit Time). There is no Read Q Time (P-Only Cycle), however, Q-Buffer 2 will be set by the I-2 and Jump signals. The data in the Accumulator now equals Read P data plus 2.

Neither Write Control will be up during Write Q Time, so no

memory currents will be active.

At Write P Time our address is still the A-Word. The Write Accumulator signal is up and we will write the accumulated data (original A-Word plus 2) into the first four bits of the A-Word.

Bit Times 5/8, 9/12, 13/16 will be identical except Q-Buffer 2 will not be set during these times. At the end of I-2 Time the MAL has been set to correspond to the A-Word address data and the original A-Word address data has been increased by 2 and written back into the A-Word.

### I-3 TIME (P&Q CYCLE)

During I-3 Time we will read the PSAR and write this data into the first register of our sub-routine. The PSAR was bumped by 2 at I-0 Time so it contains the number of the next program step of our REGULAR routine. If this data is transferred to the first Register of our sub-routine it will become an Unconditional Jump Program Step format, since there will be no data above bit 11. After our sub-routine is completed, we will use this step to Jump back to the next program step on our Regular routine.

At Read P, Bit 1/4 Time we will address the PSAR and read the first four bits. This data will be stored in the P-Buffers. The address at Read Q Time will be under control of the MAL which will contain the address of our first sub-routine register. The first four bits are read and stored in the Q-Buffer.

During Write Q Time the address remains under control of the MAL and the Write P-Buffer signal is up. The first four bits of data read from the PSAR are written into the first four bits of the first register of our sub-routine.

At Write P Time the address will be the PSAR. The Write Accumulator signal will be up and we will write into the first four bits of the PSAR. The written data will not necessarily be valid because it will be an accumulation of what was previously in the register of our sub-routine plus the data read from the PSAR. This is of no concern, however, since the PSAR will be cleared at I-0 Time before it is used again.

Bit Times 5/8, 9/12, and 13/16 will be identical to Bit 1/4 Time. During these times we will read and write the 2nd, 3rd, and 4th group of 4 bits. The first register of our sub-routine now contains an Unconditional Jump back to our main routine.

The only function remaining is to set the PSAR to address the second register of our sub-routine so we may continue through it. This is done in the remaining "I" Time.

### I-9 TIME (P&Q CYCLE)

The original A-Word contained address data of our first sub-routine. During I-3 Time this data was increased by 2 and written back into the A-Word. The A-Word, therefore, contains the address of the next Program Step to be performed. During I-9 Time we will transfer this address data from the A Word to the PSAR so that it can be used to locate the next step at I-0 Time.

At Read P, Bit 1/4 Time we will be addressing the PSAR under Clock control. Inhibit Read will be up during P Time of I—9 during the Jump operation. No data will be stored in the P-Buffer.

The A-Word is addressed at Read Q Time and the first four bits are read and stored in the Q-Buffer. The Accumulator now contains this same data since nothing is in the P-Buffer.

Neither Write Control will be up during Write Q Time, so no memory currents are active.

During Write P Time the Write Accumulator signal is up and we will address the PSAR under Clock control. The first four bits of data from the A-Word are written into the PSAR.

Bit Times 5/8, 9/12 and 13/16 will be identical except we will read and write successive 4 bit groups — clearing the PSAR of old data, reading and writing new data from the A-Word until the end of Bit 13/16 Time. The Clock will permute to I—0 Time and our Jump with Link cycle is complete.

## IMMEDIATE ARITHMETIC

At the end of I—1 Time, the Immediate Arithmetic format in the A-Word will contain the numerical data (in binary form) of some number between 0 and 255. This data will be contained in the first 8 bits. The next four bits will contain the address of some low order register (Div. by 4). The last four bits will determine the SCAT function to be performed. Two "I" Times are necessary to perform the SCAT function.

### I—6 TIME (P ONLY CYCLE)

During I—6 Time the A-Word address data (Bits 9-12) will be loaded into the MAL. Then at I—9 Time the MAL can be used to address the low order register that will be used in the SCAT function. Since this will always be a low order register divisible by 4 only Y3 through Y6 need be loaded. Load Y Instruction Time 6 signal will be up during Central Bit Time of each bit time to load Y2 — Y6. The load of Y2 will be prevented, however, by an Immediate signal condition.

During Read P, Bit 1/4 Time we will address the A-Word under Clock control. The first four bits of the A-Word will be read and stored in the P-Buffer.

No Read Q Time occurs since this is a P-Only Cycle. At Write Q Time neither Write Control will be up, so in effect nothing occurs during Q Time.

The A-Word is still being addressed at Write P Time and the Write Accumulator signal will be up. The data in the Accumulator (same as P Buffer) will be written back into the A-Word. The first four bits of the A-Word were merely read out and written back.

Bit 5/8 Time is identical to Bit 1/4. We merely read the second four bits from the A-Word and write them back in. The Load Y Instruction Time 6 signal will be up, but even if a bit is read in the last bit position (P Buffer 4) Y2 will not load because of

the Immediate signal condition on Y2, i.e., —IMM will be down.

During Bit 9/12 Time the Load Y Instruction Time 6 signal will again be up at Central Bit Time. During this time, as the 3rd four bits of the A-Word are read and placed in the P-Buffer, the P-Buffer conditions are anded with the Load Y Instruction Time 6 signal to load Y3 through Y6.

During Bit 13/16 Time the last four bits will be read at Read P Time and written back at Write P-Time to preserve the A-Word Program Step information. The I—6 cycle is complete. The MAL has been loaded to address the low order register to be used during I—9 Time and the Clock will permute to I—9 Time.

### I—9 TIME (P&Q CYCLE)

During I—9 Time the SCAT function called for by the program step will be performed. If the function is a Transfer operation the Inhibit Read Signal will be up during P Time to clear the low order register before new data from the A-Word is transferred to it. The Add signal will be up during Add and down during Subtract. The Add signal condition will affect the Accumulator inputs so data may be either accumulated at P&Q Time ( $P + Q = P$ ) if Add is up or a difference ( $P - Q = P$ ) may be obtained if Add is down (Subtract). If the function is a Compare, the Transfer of Compare signal (T+C) will be up and Add will be down.

In all cases the data to be operated upon will be contained in the first 8 bits of the A-Word. Since we only want to read the first 8 bits, the Current Source Y Log signal will be down during Q Time at Bit 9/12 and Bit 13/16 Time. No read or write currents will flow and the last 8 bits of the A-Word are not read or written.

During Read P, Bit 1/4 Time the address will be under MAL control and the low order register is addressed. The first four bits are read and stored in the P-Buffer (except in Transfer when Inhibitor Read is up).

During Read Q, Bit 1/4 Time the Clock causes an address of the A-Word. The first four bits are read and stored in the Q Buffer. The Accumulator will now contain either A-Word data only (Transfer), an accumulation of P & Q Time data (Add) or a difference between P & Q Time data (Subtract or Compare).

Neither Write control will be up during Write Q Time, so no data is written into the A-Word and the first four bits remain clear.

The Write Accumulator signal will be up during Write P Time if the function is Add, Subtract or Transfer so the accumulation (sum or difference) may be written into the first four bits of the low order register addressed by the MAL. If the function is Compare, the Write P-Buffer signal will be up at Write P Time and the original low order data (read at P Time) will be written back in the low order register.

Bit 5/8 Time will be identical to Bit 1/4 except the next four bits of the A-Word and low order register will be read and written. Remember, no Write Controls are up at Q Time so the

first 8 bits of the A-Word have been either subtracted from, added to, or transferred to the low order register, and the first 8 bits of the A-Word are now clear.

During Bit 9/12 and Bit 13/16 Time, the Current Source Y Logic signal will be down during Q Time. Therefore, the A Word data will not be read and will remain unchanged. This is done to prevent the low 8 bits of the A-Word causing a borrow or carry which affects the high order 8 bits of the low order register. The Read P and Write P cycle remains the same; however, since no A-Word data is ever added to the Accumulator, the top 8 bits of the low order register are not affected by the top 8 bits of the A-Word. The Immediate operation has now been completed and the Clock permuted to I-0 Time.

## DIRECT ARITHMETIC

The Program Step format for a direct arithmetic operation will contain two low order register addresses. The first and seventh bits (reserved for Indirect indicators) will contain zeros. Bits 2 through 6 are reserved for the first address, and Bits 8 through 12 are reserved for the second address. In a direct arithmetic operation we may either add the data in the Address 1 register to the data in the Address 2 register, subtract the data in the Address 1 register from the data in the Address 2 register (same as Compare) or we may transfer the data in the Address 1 register to the Address 2 register. The result of the SCAT function will appear in the Address 2 register except in the Compare function. In this case, the Address 2 register will be read out and rewritten with the same data. The data in the Address 1 register will always be preserved.

During I-9 Time the Address 2 register is addressed at P Time while the Address 1 register data is addressed at Q Time. These registers are sometimes respectively referred to as the P Register and the Q Register because of their I-9 Time usage.

### I-2 TIME (P ONLY)

During I-2 Time we will read the A-Word and load the MAL to locate the Address 1 Register. The A-Word data will be preserved so it will be available later.

The address during Read P, Bit 1/4 Time will be under Clock control and we will address the A-Word. The first four bits are read and stored in the P-Buffer. The Load Y signal comes true at Central Bit Time and the Y's corresponding to the bits read will be loaded.

No write controls are up during Write Q Time. The Write Accumulator signal will be up during Write P Time and the first four bits will be rewritten into the A-Word to preserve the A Word data for later use.

Bit Times 5/8, 9/12, and 13/16 will be identical. Our address will step to each group of four bits and the corresponding Y's will be loaded each Read P, Central Bit Time. Also in all cases, the A-Word data will be written back to preserve the A-Word. At the end of Bit 13/16 Time the Y's have all been loaded to match the bits read and the Clock will permute to I-5 Time.

### I-5 TIME (P ONLY CYCLE)

During I-5 Time we will use the MAL (loaded during I-2) to locate the Address 1 register and transfer the data in this register to the B-Word. The B-Word will always be clear from previous cycles. From the Arithmetic format it will be evident that we possibly loaded some of the MAL above Y6 during the preceding I-2 Time. The Address 1 Register will be a low order register and we know that only Y2 - Y6 are needed to locate a register below 32. During I-5 Time the Select Memory signal will be up during P Time, but the Select Memory Upper signal will be down. This will keep the Y's above Y6 from affecting our address decode and the decode of Y2 - Y6 will give us the proper address.

At Read P, Bit 1/4 Time our address will be under control of Y2 - Y6 and the first four bits of the Address 1 register will be read and stored in the P-Buffer.

At Write Q Time, the Write P-Buffer signal is up and under Clock control we will address the B-Word. The first four bits of Address 1 data will be written into the first four bits of the B-Word.

At Write P Time, we will again address the Address 1 register under MAL control. The Write Accumulator signal will be up and the first four bits read from the Address 1 register will be restored.

Bit Times 5/8, 9/12, and 13/16 will be identical to Bit 1/4. Each bit group of 4 will be read from the Address 1 register, written into the B-Word and rewritten into the Address 1 register. At the end of Bit 13/16 Time the Address 1 data (possibly 16 bits) will have been transferred to the B-Word. The Clock will step to I-6 Time.

### I-6 TIME (P ONLY CYCLE)

This I Time will be used to reload the MAL with the location of the Address 2 register. The A-Word (which was preserved during I-2 Time) will be read and the MAL will be loaded during Read P Time. However, during I-6 Time the Load Y Instruction Time 6 signal will be up and the regular Load Y signal will be down. The input to the Y's will be conditioned to load Y2 during Bit 5/8 Time from P-Buffer 4 and to load Y3 - Y6 during Bit 9/12 Time from P-Buffer 1, 2, 3 and 4. From the Program Step format for Arithmetic it can be seen that the Address 2 data is located in the last bit of Bit 5/8 Time and in the four bits of Bit 9/12 Time.

At Read P, Bit 1/4 Time we will address the A-Word and read the first four bits. No Y's will be loaded because of the AND conditions of the Load Y Instruction Time 6 signal.

No Write controls are up at either Q Write or P Write Time so the first four bits of the A-Word remain clear after being read.

During Bit 5/8 Time we have the possibility of loading Y2 if a bit is read in the 4th position and sets P-Buffer 4. Again no

data is written back and the second 4 bits of the A-Word are cleared.

During Bit 9/12 Time we can load Y3 – Y6 if the corresponding bits are read to set the P Buffers. No bits are written and now the first 12 bit positions of the A-Word are cleared and the Y's now contain the address data of the Address 2 register.

During Bit 13/16 Time the A-Word is merely read and cleared. There are no Y input and Load Y Instruction Time 6 conditions that will affect any of the other Y's. The A-Word will be completely clear and we will permute the Clock to I–9 Time.

#### I–9 TIME (P&Q CYCLE)

We now have the Address 1 data in the B-Word which can be addressed by the Clock. We have loaded the Y's during I–6 Time to locate the Address 2 register. During I–9 Time we will read the Address 2 register at P Time under MAL control and read the B-Word (Address 1 data) at Q Time under Clock control. We can now perform the SCAT function called for in the Program Step. Refer to the opening paragraph of this section for the data flow from Address 1 to Address 2 which will depend on the SCAT function. If we Add, Subtract or Transfer the result will appear in the Address 2 register. If we Compare, we will subtract Address 1 (B Word) from Address 2, but the original data will be rewritten into the Address 2 register from the P-Buffer instead of the normal Write Accumulator condition. If we Transfer data Inhibit Read will be up during P Time to clear the Address 2 register before new data is written in from the Accumulator.

At Read P, Bit 1/4 Time we will address the Address 2 register under MAL control (Y2 – Y6). The first four bits are read and stored in the P-Buffer (except Transfer when Inhibit Read is up).

At Read Q Time the Clock causes an address of the B-Word (Address 1 data) and we read the first four bits and store them in the Q-Buffer. The Accumulator now contains either B-Word data only (Transfer), an accumulation of Address 2 and B-Word data (Add) or a difference between Address 2 and B-Word data (Subtract or Compare).

Neither Write control will be up at Write Q Time so the first four bits of the B Word remains clear.

The Write Accumulator signal will be up at Write P Time if the function is Add, Subtract or Transfer so the accumulation (sum or difference) may be written into the first four bits of the Address 2 register. The Write P-Buffer signal will be up if the function is Compare so the original data read from the Address 2 register may be rewritten.

The same process will be repeated during Bit 5/8, 9/12, and 13/16 Times to read and write the remaining bit positions of each address. At the end of I–9 Time the Clock will permute to I–0.

## INDIRECT ARITHMETIC

In the format for Indirect Arithmetic, either or both bit positions 1 and 7 will contain a "1" instead of "0". These two bit positions are the indicator bits used to define the Indirect Operation by loading Operational Codes 6 and/or 7 during I–1 Time. The term "indirect" means that we will not perform a SCAT function on the data in Address 2 and Address 1, as we did in Arithmetic, i.e., Address 2 data plus or minus Address 1 data equals new Address 2 data. Instead, the Address 2 and/or Address 1 registers will contain the binary location of a BYTE (Half Register) of information that may only be Compared or Transferred. Depending upon the combination of Operational Codes 6 and 7 we can have Address 2 Indirect, Address 1 Indirect or both Address 2 and Address 1 Indirect. Our other choice will be Transfer or Compare (see CCU Function Chart for conclusion of I–1 Time Indirect Arithmetic). In other words, we can Transfer or Compare a 16 bit low order register (Address 1 Direct) to a Byte located by Address 2 (Address 2 Indirect). Second, we can Transfer or Compare a Byte (Address 1 Indirect) to a full 16 bit low order register (Address 2 Direct). Third, we can Transfer or Compare a Byte (Address 1 Indirect) to a Byte (Address 2 Indirect). Finally, if Operational Code 4 is on at the end of I–1 Time, the Indirect address(es) will be "bumped" by 1 so successive Bytes may be Transferred or Compared. Address 1 may be bumped at I–3 Time and Address 2 may be bumped at I–7 Time. This is accomplished by setting Q-Buffer 1 with an AND condition of Operational Code 2 & 4, Bit 1/4 Time and Instruction Time Counter conditions.

For our explanation of Indirect Arithmetic we will assume both Address 2 and Address 1 Indirect. This operation requires all available "I" Times. "I" Times 3 & 4 are used to locate the Address 1 Byte and "I" Times 7 & 8 are used to locate the Address 2 Byte. The actual transfer or compare takes place during I–9 Time.

#### I–2 TIME (P ONLY CYCLE)

During I–2 Time, we will read the program step in the A-Word, load the MAL for the Address 1 location, and preserve the A Word. This cycle is identical to I–2 of direct arithmetic. At the end of Bit 13/16 Time the Clock will step to I–3 if Address 1 is indirect.

#### I–3 TIME (P ONLY CYCLE)

This cycle is used to read the Address 1 register and transfer the data to the B-Word. The Address 1 register will be written back to preserve it. If Operational Code 4 is on (Bump) Q-Buffer 1 will be set and the address data in the Address 1 register will be increased (Bumped) by "1" as it is written back.

At Read P, Bit 1/4 Time we will read the first four bits of the Address 1 location under control of the MAL. Only Y2 – Y6 will affect our address decode. Select Memory will be up but Select Memory Upper will be down. We can only decode to a low order register. As usual, the Read P data will be stored in the P-Buffer.

The Write P-Buffer signal will be up at Write Q Time and we will address the B-Word under Clock control. The first four bits read from the Address 1 location will be written into the first four bits of the B-Word.

At Write P Time, the Write Accumulator signal is up and our address is again under MAL control (Y2 — Y6). Since this is a P Only Cycle, no data was read at Read Q Time. The data written back into the Address 1 register will be identical to the data read at Read P, unless Bump by 1 (Operational Code 4) is indicated.

During Bit 5/8, 9/12, 13/16 the process is continued until all Address 1 data has been transferred to the B-Word. Because this is an indirect operation, the Clock will step to I-4 Time. The B-Word now contains the binary location of the Byte that contains the actual data to be processed. For identification purposes, let's call this address "Byte A" since it is located by Address 1 data.

#### I-4 TIME (P ONLY CYCLE)

The B-Word which now contains the address of Byte A will be read and the MAL will be loaded to the address of Byte A. The B-Word will not be rewritten and will be clear at the end of I-4 Time.

At Read P, Bit 1/4 Time the Clock will cause an address of the B-Word. As the first four bits are read and stored in the P-Buffer, the MAL will be loaded at Central Bit Time. Y1 — Y4 will be loaded to correspond to the bits read.

No Read Q cycle occurs (P-Only). During Write Q and Write P Time our address will still be the B-Word. However, neither Write Control will be up at either Write Time and the first four bits of the B-Word are left cleared.

During Bit Times 5/8, 9/12, and 13/16 we continue reading the B-Word at Read P Time, loading the corresponding Y's and leaving the B-Word clear. Of course there are no Y's above Bit 11, but the B-Word will still be read and cleared. Remember, this is an Indirect address which means our Byte location will be above the low order registers. Therefore, we could possibly load Y1 — Y11.

At the end of Bit 13/16 Time, the B-Word has been cleared and the MAL now contains the binary address of Byte A. The Clock steps to I-5 Time.

#### I-5 TIME (P ONLY CYCLE)

The B-Word is now clear from I-4 Time. During I-5 the Byte A data (8 Bits) will be read, transferred to the B-Word and written back into the Byte A location. The Select Memory Upper signals will be up to allow the MAL decode to use all the Y's necessary to locate the Byte A.

During Read P, Bit 1/4 Time Byte A is addressed under MAL control. The first four bits are read and stored in the P-Buffer.

The B-Word is addressed by Clock control at Write Q Time and

the Write P-Buffer signal is up. The first four bits are written into the B-Word.

At Write P Time, we will again address Byte A with the Write Accumulator signal up. The first four bits are written back into Byte A to preserve them.

At P and Q Time of Bit 5/8, the second group of 4 bits will be transferred from Byte A to the B-Word and rewritten into Byte A. Our 8 bits of data have now been transferred.

During Bit 9/12 and 13/16 Time, the Current Source Y Logic signal will be down to prevent reading and writing the next 8 bits (Byte). The cycle will be complete and the Clock steps to I-6 Time.

#### I-6 TIME (P ONLY)

This cycle is identical to the I-6 Time of direct arithmetic. The A-Word will be read at Read P Time and the MAL will be loaded. Y2 will be loaded from P-Buffer 4 at Bit 5/8 Time and Y3 — Y6 will be loaded from P-Buffer 1, 2, 3, 4 at Bit 9/12 Time. At the end of this cycle the A-Word will be clear and the MAL (Y2 — Y6) will contain the binary location of the Address 2 register.

#### I-7 TIME (P ONLY CYCLE)

Using the MAL Y2 — Y6 the Address 2 register will be read and its data (Binary location of the Byte that contains the actual data to be transferred or compared) will be written into the A-Word. The A-Word was cleared at the end of I-6 Time. The Address 2 register will be rewritten with its original data or bumped by 1 if Operational Code 4 is on.

At Read P, Bit 1/4 Time the address will be under MAL control (Y2 — Y6). The first four bits of the Address 2 register will be read and stored in the P-Buffer. Q Buffer 1 will be set during Bit 1/4 Time if Operational Code 4 is on to add "1" to the Accumulator total (P-Buffer + 1).

At Write Q Time, the A-Word is addressed by Clock control and the Write P-Buffer signal is up. The first four bits of Address 2 data will be written into the first four bits of the A Word.

At Write P Time, the MAL will again address the Address 2 register. The Write Accumulator signal will be up. Either original data or original data plus "1" will be written back into the first four bits of the Address 2 register.

Bit Times 5/8, 9/12 and 13/16 will follow the same sequence except no bump by one will occur. At the end of Bit 13/16 Time the Address 2 data has been transferred to the A-Word and rewritten into the Address 2 register in its original form or plus 1 if bumped.

The A-Word now contains the binary location of the Byte that contains our data to be transferred or compared at I-9 Time. For identification purposes, let's call this address BYTE B since it was located with the Address 2 register. The Clock will step

to I-8 Time at the end of this cycle.

#### I-8 TIME (P ONLY CYCLE)

With the Byte B Address in the A-Word, we can now read this Address and load the MAL to its location. At the end of I-8 Time data at both of the Indirect locations will be available for calculating at I-9 Time. The data from Byte A has been transferred to the B-Word (I-5 Time) which can be addressed by Clock control and the MAL can be used to address the Byte B data.

At Read P, Bit 1/4 Time the A-Word is addressed by Clock control. The first four bits are read and stored in the P-Buffer. The Load Y signal will be up at Central Bit Time to load the Y's corresponding to the bits read.

Neither write control is up at Write Q Time.

The Write Accumulator signal is up at Write P Time and the A-Word is rewritten. This is a redundant operation since it is not necessary to preserve the A-Word. It is allowed since it creates no problem and would require additional circuitry to prevent.

#### I-9 TIME (P & Q CYCLE)

The actual Transfer or Compare operation will take place at I-9 Time. Refer to the opening paragraph of this section for the possible combinations of Indirect operation. In our example, we assumed both Address 2 and Address 1 as Indirect. This means we will be Transferring or Comparing a Byte (8 Bits) to a Byte. The Byte defined by Address 1 (Byte A) is in the B-Word. The Byte defined by Address 2 (Byte B) will be located with the MAL loaded during I-8 Time. We are above the low order registers so Y1 - Y11 will be used to decode the address of Byte B. Select Memory and Select Memory Upper will be up during P-Time, Select Memory Upper will AND with - Inst. Time 1, - Jump and Bit Counter B to kill the CSY Logic during Bit 9/12 and 13/16 Time. Therefore, only 8 Bits will be read or written during P-Time when Address 2 is indirect.

At Read P, Bit 1/4 Time the Address 2 Indirect location (Byte B) will be addressed by the MAL. The first four bits are read. In a Compare cycle this data is stored in the P-Buffer. If the cycle is Transfer, Inhibit Read will be up during P Read and no data will reach the P-Buffer.

During Read Q Time, the B-Word is addressed. The B-Word contains the Byte A data. The first four bits are read and stored in the Q-Buffer. The Accumulator will now contain either Read Q data (Transfer) or a difference between Read P data and Read Q data (Compare).

Neither write control will be up at Write Q Time, so the B-Word will be cleared by not being rewritten.

At Write P Time, we will write from the P-Buffer in a Compare cycle or from the Accumulator in a Transfer cycle. We will be addressing Byte B under MAL control. In a Compare operation the data in Byte B is written back unchanged. In either case the B-Word is left clear for the next Program Step.

Bit 5/8 Time is identical and the next 4 bits of each Byte are read and written.

The Current Source Y Logic will be down during Bit 9/12 and Bit 13/16 Time so no read or write currents flow during P Time. However, the B-Word will still be read and not rewritten during Q Time.

At the end of Bit 13/16 Time, our 8 bits of data from each Indirect location have been operated upon and the Clock will permute to I-0 Time to begin the next Program Step.

#### PROGRAM CONTROL

The format for Program Control will define a low order register and a single bit within that register. Operational Codes 5 and 6 will be used in combination to determine whether the bit defined will be set, reset or preserved. The MAL will be loaded to correspond to the register and bit. Y2 - Y6 will be used to locate the register, Y8 - Y9 will locate the bit position in a bit group located by Y10 - Y11. Refer to the CCU Function page in the reference section for a chart of the Y combinations. Y8 - Y11 combined with Operational Codes 5 and 6 will control the sense-inhibit lines to set, reset or preserve the particular bit. As the bit is sampled (read), its state will be used to set or reset the Low and Equal latches.

#### I-2 TIME (P ONLY CYCLE)

During I-2 Time, the A-Word will be read and the MAL (Y1 - Y11) will be loaded to correspond to the bits read.

At Read P, Bit 1/4 Time we address the A-Word under Clock control and read the first four bits. With this data in the P-Buffer, the Load Y signal is up at Central Bit Time to load the corresponding Y's.

No write controls are up during Write Q Time. The Write Accumulator signal is up during Write P Time and the original data (P-Buffer plus 0) will be written back into the first four bits of the A-Word.

Bits 5/8, 9/12, 13/16 will be read, the Y's loaded and the data restored in the A-Word. At the end of Bit 13/16 Time the MAL has been loaded and the A-Word completely restored. The Clock will step to I-3 Time.

#### I-3 TIME (P ONLY CYCLE)

The bit within the defined register will now be sampled (read) and its state used to set or reset the Low and Equal latches. We will also have the ability (under control of Operational Code 5 & 6) to either set, reset or preserve this bit position. Y10 and Y11 will be ANDED with Clock Bit Counter conditions to generate a signal called SAMPLE BIT TIME during the bit time defined by the Y10 and Y11 conditions. The Y8 and Y9 conditions which define the actual bit are ANDED with the Accumulator outputs to control the signal SAMPLE BIT POSITION. If the Accumulator output corresponding to the Y8 and Y9 conditions is down at I-3, Write P Time, Sample Bit Position will be up and the Low latch will be set. The Low latch will in turn reset the Equal latch. If the Accumulator out-

put corresponding to the Y8 and Y9 conditions is up at I-3, Write P Time, Sample Bit Position will be down and the Low latch will remain reset and Equal latch will remain set. The states of these latches can then be used to alter the program routine.

During each Read P, Write Q, Write P Time the MAL (Y2 - Y6) will address the desired register. It will be read at Read P Time and each 4 bit data group will be stored in the P-Buffer. No Read Q occurs so the Accumulator will contain identical data. The bits will be read and written back except when the Sample Bit Time and Sample Bit Position conditions are true for the one bit position located by Y8, Y9, Y10, Y11. This bit may either be left in its original state (rewritten), reset to zero or set to a "1" depending on the Operational Code 5 and 6 combinations which will control the memory Current Source pertaining to that bit position.

At the end of Bit 13/16 Time, the Clock will permute to I-0. The state of the Low and Equal latches can now be used to alter the regular program routine if necessary.

### INCREMENTAL JUMP

The format for Incremental Jump (actually an Arith. Operation) will define one of the special registers (16, 24, 48, 56), a bit within that register and the increment to be jumped forward or backward. Operational Code 3 will denote whether to jump forward or backward by controlling the add/subtract cycle at I-9 Time. Operational Code 3 "on" will denote forward (add increment) while Operational Code 3 "off" will denote backward (subtract). Operational Code 5 will determine whether we jump with the defined bit "on" or "off". With Operational Code 5 on, we will take the jump if the bit is on. With Operational Code 5 off, we will take the jump if the bit is off. The output of Operational Code 5 is ANDED with the output of the Low and Equal latches which are set when the defined bit is read. If the bit is "on" Equal will be set "on"; if the bit is "off" Equal will be reset "off". Actually, the programming choice is to jump or not jump, depending on the state of the Equal latch. If the proper conditions are true, TAKEN will come up and we permute to I-9 and add or subtract the increment amount to or from the PSAR.

We have the ability to jump forward up to 16 registers (prog. steps) or backward as many as 14 with reference to the initiating program step. At the end of I-0 Time, the PSAR has already been bumped by 2 and if maximum increment was used (binary total of 30) our PSAR net increase would be 32 at the end of I-9 Time. This means we would then move up 32 Bytes or 16 program steps since each program step takes a full register (2 Bytes). We could also subtract 30 from the PSAR but it has already been bumped by 2 at I-0 so our net reduction would actually be 28 or 14 program steps backward.

### I-2 TIME (P-ONLY CYCLE)

We will use this "I" Time to read the A-Word and load the MAL to locate the special register (16, 24, 48 or 56) and to define the particular bit in this register so it can be sampled. The A-Word will be rewritten except bits 6, 7 and 8 (Bit 5/8 Time).

If Bit 5 was on when read it will be written back. This leaves only "increment" data in the first Byte of the A-Word.

At Read P, Bit 1/4 Time we will address the A-Word under Clock control. The first four bits are read and Y1 - Y4 are loaded from the P-Buffers at Load Y Time.

No write control is up at Write Q Time. The Write Accumulator signal will be up at Write P Time and the first four bits are written back into the A-Word.

At Read P, Bit 5/8 Time, a signal called Incr. Jump Reset Y will be up. This signal will reset Y2, Y3 and Y4 (notice from format that Y1 could not be set at Bit 1/4 Time). The second bit group will be read and stored in the P-Buffer. When the Load Y signal comes up, Y5, Y6, Y7 and Y8 will be loaded from the P-Buffer. Operational Code 1 and "I" Time Counter B are both true, so Y5 will be set even if P-Buffer 1 is off. Y4 will be set by Bit 5/8 and P-Buffer 3, therefore bit position 7 loads Y4. Now Y4, Y5 and Y6 define the register to be addressed. Binarily Y4 = 8, Y5 = 16, and Y6 = 32.

During Write P Time, the Write Accumulator signal will not be up. A special Current Source 1 condition, however, will write the 5th bit back if Accumulator 1 is on during Bit 5/8 Time of Incremental Jump. This bit must be preserved if on when read because it is part of our increment data.

MAL Y9, Y10 and Y11 will be loaded during Read P, Bit 9/12 Time from the normal Load Y and P-Buffer conditions. The Write Accumulator signal will be up at Write P Time and these bits will be written back into the A-Word.

During Bit 13/16 Time, the remaining four bits are read and written back.

At the end of I-2 Time, the Y's have been loaded to define the Special Register and bit. The first 8 bits of the A-Word now contain only the increment data since we did not write during Bit 5/8 Time (except possibly the 5th bit). The Clock will step to I-3 Time.

### I-3 TIME (P-ONLY CYCLE)

The selected special register will be read during I-3 Time and the particular bit will be sampled to determine if the condition in the format has been met. Taken will come up if the sampled bit matches the jump on Equal, jump on Not Equal choice. The Low and Equal latches will be set and compared to Operational Code 5 to develop this Taken signal. If Taken comes up, we will permute to I-9 to update the PSAR; if not, we will permute to I-0.

At Read P, Bit 1/4 Time, the address is under control of the MAL. The Select Memory Upper signal is down, so only the Y2 - Y6 combination will be used in the decode of the special register (16-24-48-56). The first four bits are read and stored in the P-Buffer.

The Write Accumulator signal is up at Write P Time and the special register is rewritten.

Bit 5/8, 9/12 and 13/16 Time are identical. The other bit groups are read and rewritten.

During the Read P portion of each bit time, the condition of Y8, Y9, Y10, Y11 will be defining a particular bit group and bit within that group. As the selected bit is read, the Accumulator output is used to set the Low and Equal latches to match the bit condition. Then the Low and Equal outputs will develop Taken if the program conditions are met. If Taken comes up, we will permute to I-9 Time.

#### I-9 TIME (P & Q CYCLE)

The increment data in the A-Word will be added to or subtracted from the PSAR during I-9 Time. Whether we add or subtract will depend on Operational Code 3. If jump forward we add, if jump backward we subtract.

At Read P, Bit 1/4 Time, we will address the PSAR under Clock control. The first four bits will be read and set in the P-Buffers.

At Read Q Time, we will address the A-Word and read the first four bits and set them in the Q-Buffer. The Accumulator will now contain a sum or difference of the two registers.

We will not write at Write Q Time because neither write control is up. This will leave the first four bits of the A Word clear.

At Write P Time, we will write the sum or difference into the first four bits of the PSAR.

During Bit 5/8 Time, the second four bits of the PSAR and the A-Word are read and the sum/difference written into the PSAR.

The Current Source Y Logic signal will be down during Q Time of Bits 9/12 and 13/16 to prevent reading and writing the A-Word. All increment data was in the first 8 bits of the A-Word and has been used to update the PSAR. The remaining data in the A-Word must not be used or the PSAR would be incorrectly updated. The PSAR is read at Read P and written at Write P during Bit 9/12 and 13/16. No Q data will be added because of the CSY Logic signal being down.

At the end of I-9 Time, the PSAR will contain the next program step to be performed and the Clock will permute to I-0 Time.

#### INPUT

Data may be inputted from either the Magnetic Tape Reader, the Paper Tape Reader or the Console Keyboard. The Program Step format contains this input choice and the memory location (low order register) where the data will be stored. Data from all input devices will pass through the P Buffers before being written into the memory location. If the data is from the MT or PT Reader, an Input Strobe signal will be used to set the P-Buffers. If data is from the Console Keyboard a Keyboard Entry signal will be used to set the P-Buffers. In either case, this data is set in the P-Buffers and written into memory dur-

ing I-5 Time. One other "I" Time, I-2, is used to load the MAL to locate the input register and define the input device. Y2 - Y6 will define the memory location (low order register) and Y8, Y9 and Y10 will define the input device. Y11 defines the input devices station, i.e., right or left, number one or two, etc. These Y's are loaded from the A-Word during I-2 Time.

#### I-2 TIME (P-ONLY CYCLE)

As stated above, the MAL will be loaded from the A-Word during this "I" Time. During P Time, we will address the A-Word under Clock control. The A-Word will be restored by writing from the Accumulator during Write P Time. During each Read P Time, four bits will be read and the corresponding Y's set when Load Y comes up. As can be seen from the format, Y1 and Y7 will never be loaded since these bit positions will always contain zeros. Only direct input program steps are defined.

No write controls are up at Write Q Time. The Write Accumulator signal is up at Write P Time and the A-Word is rewritten with its original data. At the end of Bit 13/16 Time the Y's are loaded and the A-Word restored. The Clock will permute to I-5 Time.

#### I-5 TIME (P-ONLY CYCLE)

Data read from either Tape Reader device will be stored in the Input Data Latches (see Tape Reader section). The Device Code signal defined by Y8, Y9 and Y10 will be ANDED with the Data Latches to define the Bit codes.

During Read P, Bit 1/4 Time, the low order register (Y2 - Y6) will be addressed and the first four bits read. Inhibit Read will be up to prevent any data read reaching the P-Buffers. The first four bits are now clear. When Central Bit Time comes up during I-5 Time of an Input Step, the Input Strobe signal comes up. Input Strobe will AND with the Bit outputs and set the corresponding P Buffers. The P Buffers now contain the first four bits read from the tape.

At Write Q Time, the Write P-Buffer signal is up and at Write P Time the Write Accumulator signal is up. We will therefore write the same data into the same location (low order register Y2 - Y6) twice. This is of no consequence, and is merely a redundant cycle that would take additional logic to overcome. The first four bits have been written into memory.

During Bit 5/8 Time, the next four bits are transferred from the P-Buffers to the low order register. Each character consists of an 8 bit code so the input character has been transferred from the Input Data Latches via the P-Buffer to the assigned register.

The top 8 bits of the assigned register will be read during the following Read P cycles of Bit 9/12 and 13/16. The P-Buffers will not be set so nothing is written during the Write Q, Write P portions of these bit times. The last 8 bits of the low order register remain clear.

At Bit 13/16, Input Strobe Time, a signal called Read Com-

mand will come up. The Read Command signal will indirectly repick the cycle clutch in the Input Device to read the next character into the Data Latches.

If no character is stored in the Data Latches when an Input Program Step is called for, the signal Character Ready will be down. At I-2, Bit 13/16 Time, the Pre-Inhibit latch will set because Character Ready is down. Then with Pre-Inhibit set, the Inhibit latch will set at the beginning of I-5 Time. The selected register will be addressed and cleared at I-5 because there will be no data transferred to the P-Buffers if there is no character in the Data Latches. The Clock will permute to I-0 as usual to perform the next program step. However, the present step wasn't successfully performed because no character was ready. We must repeat this same step over and over until a character is ready and is written into our selected register at I-5 Time. Only then can the program process continue.

With Inhibit up, the bump by "2" will be prevented during the next I-0 Time. The MAL will be loaded to our old program step plus 2 since we did bump during our original I-0 Time. This is O.K., however, because at I-1 Time, Inhibit will cause Select A-Word to be up during the complete I-1 Time. We merely read the A-Word and write it back. The MAL is not used to control our address. Remember, the A-Word still contains our present program step (Input) so the Operational Codes will be reloaded again and the previous Input cycle will be repeated. During I-1, Bit 13/16, Write time Upset Pre-Inhibit will come up and will reset the Pre-Inhibit latch at Steer Latch Strobe time. With the Pre-Inhibit latch off, the Inhibit latch will be reset at I-2, Read time. With Inhibit down, a normal I-2 and I-5 Time will be performed if a character is ready and our input step is complete. However, if a character still isn't ready (-Character Ready up), Pre-Inhibit will come up at I-2, Bit 13/16 Time and cause Inhibit to be set again at the beginning of I-5 Time and our Inhibit cycle will be repeated until a character is finally ready.

INPUT FROM KEYBOARD (Normal)

If the program step is an Input from Control Panel step we will follow basically the same procedure as stated above for Input from the Readers. The same "I" Times will be used. I-2 Time will be used to load the MAL to the address of the low order register and I-5 Time will be used to transfer the entered data from the P-Buffer to the defined low order register.

In order to repeat the step until some data is entered, the programmer will use the condition of the Equal latch. The Equal latch will be on at the beginning of the program step. To generate the Reset Equal signal requires a Keyboard Strobe signal ANDED with Not Edit and Not Accumulator Equal Zero. This means the Equal latch will remain on until non-zero data is entered. If the next program step is a Jump on Equal back to this Input step the CCU will "loop" between these two program steps until the Equal latch is reset by a non-zero entry.

When one of the Keybuttons is depressed its contacts are integrated to produce Keyboard Code Ready and a decode of Keyboard Contacts A, B, C, D. The various decode signals are shown in the chart below. For reference, Key number 1 is Line

Stop, the last key on the right side of the keyboard and Key number 12 is the Start key.

KEYBOARD CODE LOGIC

KEY	A	B	C	D	KB CDE RDY
1			x	x	x
2	x				x
3		x			x
4	x	x			x
5			x		x
6	x		x		x
7		x	x		x
8	x	x	x		x
9				x	x
10	x			x	x
11		x		x	x
12	x	x		x	x

Keyboard Code (defines Console) is ANDED with Input, I-5, Central Bit Time to bring up Keyboard Strobe. The Keyboard decode logic is ANDED with Bit Times 1/4, 5/8, and 9/12 to bring up Keyboard Bit Group. Keyboard Strobe, Keyboard Code Ready and Keyboard Bit Group will bring up Keyboard Entry Strobe to AND with the Keyboard Code (A, B, C, D) combinations to load the P-Buffer corresponding to the depressed keybutton.

During I-5 Time the P-Buffer data is written into the defined low order register. This portion of the cycle is identical to I-5 Time of Input from the Readers.

Any data set in the P-Buffer will also enter the Accumulator. When the first bit is entered, the Accumulator Not Equal to Zero signal will go up. This signal is ANDED with Not Edit and Keyboard Strobe to bring up Reset Equal and the Equal latch is reset (turned off). With Equal reset, the Jump on Equal step mentioned previously will not be performed and the program routine will continue.

Considering the speed of the CCU compared to depressing and releasing a keybutton, it is evident that some means must be taken to prevent more than one input step per keybutton depression. This is accomplished by bringing up Inhibit to prevent the program sequence from progressing until the keybutton is released.

The Reset Equal signal will also set a latch called Keyboard

Single Entry. This latch will remain set until the keybutton is released. Keyboard Single Entry is ANDED with Input to set the Pre-Inhibit latch when Upset Pre-Inhibit comes up at the next I-1, Bit 13/16, Write Time. With Pre-Inhibit on, Inhibit will set at I-2 Time. Inhibit will prevent the program routine from progressing until the keybutton is released. When the keybutton is released, Keyboard Common will come up and reset Keyboard Single Entry. With Keyboard Single Entry down, Pre-Inhibit and Inhibit will not set during the next I-1 and I-2 Times and the program step routine will continue.

So far we have covered what might be considered "normal" input from the keyboard — that is, input from the keyboard while the CCU is under control of the regular Composition program. Examples of this type input include set-up entries such as clear yes or no, measure, minimum interword space, etc.

### INPUT FROM KEYBOARD (EDIT)

The Customer Engineer may also enter data into the CCU by placing the CE test switch in the Edit Address or Edit Data positions. This procedure is explained in the Reference Manual under Diagnostics.

### INPUT FROM KEYBOARD (LINE STOP)

Depressing the Line Stop keybutton during normal CCU operation will terminate the program routine. The program routine stops in the set-up mode and the output device stops after the last inputted line has been printed. We will not be concerned with the program technique involved, except to understand that before each new line is inputted, a check will be made to see if there has been a Line Stop entry. This check will include an input step.

Depressing the Line Stop keybutton will bring up the integrated signals Keyboard Code C and D. These two signals AND with NOT Keyboard Single Entry to set the Line Stop latch. At I-5, Central Bit Time of the Input step (see paragraph above) Keyboard Strobe will turn on. Keyboard Strobe and Line Stop latch will turn on Keyboard Entry Strobe during Bit 1/4 Time. Keyboard Entry Strobe and Keyboard Codes C and D will cause P-Buffer 1 to set (—A—B conditions). The Accumulator will also contain a "1" and Accum. Not Equal to Zero will bring up Reset Equal which sets Keyboard Single Entry.

The P-Buffer data (1 Bit) will be written into memory during Bit 1/4 (see normal input explanation) of this same I-5 Time. The Line Stop latch is reset at Bit 5/8 Time.

If the Line Stop Keybutton has not been released before the next Input step (console) occurs, Pre-Inhibit will set at I-1, Bit 13/16 Time from Upset Pre-Inhibit, Input and Keyboard Single Entry. Remember, once Keyboard Single Entry sets, it will not be reset until the keybutton is released to bring up Keyboard Common. Pre-Inhibit will cause Inhibit to set at I-2 Time to "hang up" the program as usual.

When the Line Stop keybutton is released, Keyboard Common will reset Keyboard Single Entry. Pre-Inhibit and Inhibit will

not come back up during the next I-1 and I-2 Times and the interrupted Input program is completed. However, since the Line Stop latch was reset during Bit 5/8 Time at the first input step, no data is written since P-Buffer 1 will not be set during this I-5 Time.

### OUTPUT

The format for Output will define the location of the character in memory and the device to which this character is to be outputted. Two types of Outputs are available. Normal Output refers to transferring one Byte from Memory to the Output Register. This may be either a direct or indirect address operation. Our second choice is overlapped or Multiplex Output. In a Multiplex operation, the program sequence is interrupted each time the output device is ready to accept another character until a block of Bytes (line of type) is outputted.

A normal direct output requires one "I" Time (I-2) to load the MAL and one "I" Time (I-5) to load the Output Latches. An indirect Output will require two additional "I" Times (I-3 and I-4) to load the MAL with the indirect address.

### I-2 TIME (P-ONLY CYCLE)

During I-2 Time the program step will be read from the A-Word, the MAL will be loaded and the A-Word will be preserved. At the end of I-2 Time the MAL will contain a low order address (Y2 — Y6) and the output device code (Y8 — Y10). If Multiplex was programmed, Y11 would be loaded to define Multiplex.

At Read P, Bit 1/4 Time we will address the A-Word under Clock control. The first four bits are read and set in the P-Buffer. When the Load Y signal comes up at Central Bit Time the first four Y's will be loaded to correspond to the bits read.

Neither Write Control will be up during Write Q Time. The Write Accumulator signal comes up at Write P Time and we are again addressing the A-Word. The first four bits of the A-Word are restored.

During Bit 5/8, 9/12, and 13/16 Times the above routine is repeated to read the other bit groups, load the corresponding Y's and restore the A-Word.

If Operational Code 6 is up (indirect) the Clock will step to I-3 Time. If Operational Code 6 is down (direct) the Clock will permute to I-5 Time.

### I-3 TIME (P-ONLY CYCLE)

During I-3 Time the indirect address (Byte) will be transferred to the B-Word. Q-Buffer 1 will be turned on during Bit 1/4 Time to add 1 to this address. The sum will be written into the original memory location. In a Multiplex operation this will be Register 0.

At Read P, Bit 1/4 Time we will address the low order memory location under Y2 — Y6 Control. The first four bits are read and set in the P-Buffer.

There is no Read Q Time (P-Only); however, the B-Word will already be clear from a previous cycle. Q-Buffer 1 will be turned on at Bump Strobe Time to add 1 to the Accumulator.

The B-Word is addressed at Write Q Time and the Write P Buffer signal is up. The first four bits of data read at Read P Time are written into the B-Word.

At Write P Time we will again address the memory location under Y2 — Y6 Control. The Write Accumulator signal will be up and the accumulated data (Read P + "1") will be written into the first four bits of the memory location.

During Bit 5/8, 9/12, and 13/16 Times the same process is repeated except Q-Buffer 1 is not turned on during these times.

The original memory location (low order register) data has been bumped by 1 and the B-Word now contains the address of the Byte to be outputted.

#### I—4 TIME (P-ONLY)

The B-Word will be read and the MAL will be loaded to define the address of the Byte to be outputted. The B-Word will not be restored and will be clear at the end of I—4 Time.

At Read P, Bit 1/4 Time the B-Word is addressed under Clock Control. The first four bits are read and set in the P-Buffer. The Load Y signal will be up at Central Bit Time to load the first four Y's to correspond to the bits read.

Neither Write Control is up during Write Q or Write P Time and the first four bits of the B-Word will remain clear.

The same procedure follows during Bit 5/8, 9/12 and 13/16 Time as the remaining bit groups are read and the rest of the Y's are loaded.

The MAL now contains the address of the Byte to be outputted and the B-Word has been cleared.

#### I—5 TIME (P-ONLY CYCLE)

During I—5 Time the Byte containing the character to be outputted will be read and the Output Latches will be loaded. The address of the Byte will be defined by Y2 — Y6 in a direct operation and by Y1 — Y11 in an indirect operation. All characters are made up of 8 bit codes, therefore, the Current Source Y logic signal will be down during Bit 9/12 and 13/16 Times to prevent reading erroneous information.

At Read P, Bit 1/4 Time we will address a Byte in memory under MAL Control. Either the Y2 — Y6 or Y1 — Y11 combination will be used depending upon Operational Code 6. This Operational Code (loaded at I—1 Time) will define whether we are using a direct or indirect output operation. The first four bits are read and stored in the P-Buffer. At Central Bit Time the Load Output Latch signal will come up if the output device is ready. The Load Output Latch signal is ANDED with Bit 1/4 and the P-Buffer outputs to load the first four Output Latches. Note that the RESET Output Latch signal also has the

Bit 1/4 Load Output Latch conditions plus Clock signal B. This means the Output Latches will be reset just prior to being loaded. However, load will override reset if the same Output Latch is being reloaded. Note also that both the load and reset signals depend on the feedback signal READY. This feedback signal insures that the Output Latches will not be reloaded with a new character until the previous character has been operated upon by the output device and it is "ready" for the next one.

During both Write Q and Write P Times our address is under MAL Control. The Write P-Buffer signal is up during Write Q Time and the Write Accumulator signal is up during Write P Time. The Accumulator and P-Buffer contain identical data since there was no Read Q Time. The first four bits of data are written back into memory twice. This presents no problem, however, since the same data is written each time.

The second bit group will be read at Bit 5/8 Time and the Output Latches loaded accordingly. The Load Output Latch signal will be ANDED with the Bit 5/8 signal and P-Buffer outputs to load the second four Output Latches. Remember all of the Output Latches were reset at Bit 1/4 Time, so these last four are clear and ready to be loaded prior to Bit 5/8 Time. There is no need for an additional reset during Bit 5/8 Time.

All 8 Output Latches have now been loaded and the memory Byte written back with the original data. No further reading and loading is necessary. During Bit 9/12 and Bit 13/16 Time the Current Source Y logic signal will be down to prevent reading erroneous information from the next Byte.

The Output Latches are now loaded and we are ready to output either to the Console Lights or to the Translator depending upon the Program Step format. Let's consider the Lights first.

#### OUTPUT TO LIGHTS

During I—2 Time Y8, Y9 and Y10 would have been loaded from the "output device" portion of the program step format and bring up a signal called Keyboard Code. The Select Output Device Signal would also come true at I—2 Time during a normal output (Multiplex down) because Ready would be up. Since no feedback is required on the Lights (non-mechanical) they are always considered ready to accept a character (Byte). Select Output Device and Keyboard Code will turn on the Lights latch and bring up the Output Register signal. The Output Latch signals are ANDED with the Output Register signal to turn on our light drivers and lights corresponding to the Output Latch conditions.

#### OUTPUT TO TRANSLATOR (NORMAL)

Assume we are in a normal Output to Translator Program Step. The Output Latches have been loaded with a character and we are in I—5 Time ready to pick the Translator cycle clutch and selection magnets. The Translator will produce a pull on one of the keylever links and a Composer cycle will result.

First, let's consider the sequence of operation assuming both units are at rest at the beginning of the output step, ready to

accept a character from the CCU.

## TRANSLATOR READY

If the program step format called for an output to the translator, neither Y8, Y9 or Y10 would have been loaded during I—2 Time. Assuming this is not a Multiplex operation (Y11 down) Select Output Device will be up at I—2 Central Bit Time with the Translator at rest (Ready up). Select Output Device is ANDED with the NOT conditions of Y8, Y9, and Y10 to set the Translator Select Latch. With the Translator ready (Ready is up), the Busy latch will set at I—5, Bit 13/16, Steer Latch Strobe Time. As soon as Busy sets, Ready will be reset. Busy is ANDED with Translator Select plus the feedback signals from the Translator to bring up Translator Print. Translator Print ANDS with a Not Master Reset and Not Sync 1 condition to turn on the magnet driver for the Translator cycle clutch. Translator Print is also ANDED with the Translator selection magnet contact signal (SEL. MAGS.) and the Output Latch signals to energize the translator selection magnets corresponding to the character in the Output Latches.

## TRANSLATOR CYCLE

As the Translator begins its cycle, the Translator Cycle Clutch contact will transfer at approximately 65 degrees. The N/O contact produces the integrated signal Cycle Clutch N/O which will set (turn on) the Output Interface Feedback latch. Output Interface Feedback will cause Busy to be reset (turned off) at the next Central Bit Time. NOT Output Interface going down will turn off Translator Print to drop the Translator cycle clutch and the Selection Magnets.

At 280 degrees of the Translator cycle the Cycle Clutch N/C contact will remake. The Cycle Clutch N/C integrated signal will reset (turn off) the Output Interface Feedback latch. NOT Output Interface Feedback will come up and reset the Output Interface Feedback\* latch.

We now have Busy off and Output Interface Feedback\* off. With the NOT outputs of both of these signals up, the Ready latch will be set at the beginning of the next I—0 Time when Begin Program Step comes up. It must be remembered that at the end of I—5 Time of the Output program step the Clock permuted to I—0 Time and the next program step was begun. The CCU could have performed many program steps during the time it has taken the mechanical units to cycle this far.

With the Busy latch off and the Ready latch on the Translator is now ready to accept another character from the CCU. At 335 degrees the N/O Selection Magnet contact will remake and the Translator Selection Magnets may be energized for the next Output to Translator cycle. However, the Output Latches will not be reset until the Load Output Latch and Reset Output Latch signals come up during I—5 Time of the next Output program step.

## TRANSLATOR BUSY

Should another Output program step occur before the Translator has completed the first cycle, this new step must be pre-

served until the Translator is again ready. This is accomplished by the feedback signals from the Translator which ultimately control the Ready and Busy signals.

Referring to I—5 Time of our previous Output step we see that Busy was turned on to initiate the Translator cycle and to turn off the Ready signal. It can also be seen that Busy is not turned off until after 65 degrees and Ready is not turned back on until late in the Translator cycle — after 280 degrees.

If another Output step occurs before Ready is turned back on, Output and Not Ready will cause Pre-Inhibit to set at I—1 Time of the new Output step. With Pre-Inhibit on, Inhibit will set at the beginning of I—2 Time of the new Output step. With Inhibit up the CCU will be forced to repeat the Output step and preserve it in the A-Word until the Translator is ready for another character. Refer to the previous section for explanation of how this is accomplished.

Ready being down will prevent Select Output Device coming up at I—2 Time. It will also prevent the Load and Reset Output Latch signals. In other words, we cannot set up the pick of the Translator cycle clutch or dump the previous character in the Output Latches and load another one until the Translator is ready for the new character.

The CCU will repeat the new Output program step until the Translator cycles past 280 degrees. Busy has already been turned off (around 65 degrees), and Output Interface Feedback\* will turn off after 280 degrees. The next I—0 Time will turn Ready on (Begin Program Step Time). With Ready on, Pre-Inhibit and Inhibit will not be set, the new Output step will be performed and the program step sequence continues.

## OUTPUT TO TRANSLATOR (MULTIPLEX)

So far our discussion has been limited to Normal Output which refers to outputting one character (Byte) per program step. Our second choice, Multiplex Output, refers to initiating the outputting of a block of characters (Bytes) with one program step, while allowing the regular Composition program to continue anytime the Translator is busy with a character. Once the Multiplex step has been initiated, it will continue until a HALT code is read. The Halt code is the programmer's responsibility and will be installed at the end of each block of characters. For illustration, let's assume the Translator is idle when the Multiplex step is read and follow the CCU and Translator cycles:

1. The Multiplex program step is read, the Multiplex latch sets, and the first character is transferred to the Output Latches. This is basically a normal indirect output step with Register 0 always containing the indirect address data. Register 0 will be bumped by 1 to update the address data for the next character (Byte).
2. Busy is turned on to pick the Translator cycle clutch to output the first character. Ready is turned off. The Translator is now "busy". At the end of I—5 Time the Clock will permute to I—0 and the next program step is read.

3. With Multiplex up and Ready down, the CCU will continue performing the Composition program steps until the Translator completes its operation on the first character and Ready comes up again.
4. With Ready up and Multiplex still up, the Composition program routine is interrupted. Multiplex will turn on the Operational Code Latches to define an Indirect Output Step. The MAL will be reset to define Register 0 and the second character will be transferred to the Output Latches using the Register 0 indirect address. This address is again bumped by 1 to locate the third character for the next Output step. Inhibit will be turned on to preserve the interrupted Composition Program Step.
5. This routine will continue (Items 2—4) until a Halt Code is read to reset the Multiplex Latch and terminate the operation.

Multiplex output is limited to one output device. With the Multiplex latch set, Select Output Device cannot be turned on to identify another device. If a normal Output step is read while the CCU is performing the Composition program steps during the Multiplex operation, the Inhibit function will preserve the step in the A-Word as usual. However, Output and Multiplex will cause Pre-Inhibit to set at each I—1 Time because Output will be up during Multiplex Output or normal Output. Inhibit will set each I—2 Time, therefore, the normal Output step cannot be performed until Multiplex is turned off by the Halt Code. This means the CCU Composition program will “hang up” on the normal Output step until the entire block of Multiplex characters has been outputted.

With an overall picture of the operation in mind, let's go back and examine the “I” Times of each program step situation more closely. You will notice the first program step explanation is identical to any indirect output program step except the Multiplex latch is set during I—2 Time and the indirect address data will always be in Register 0. However, this will serve as a review of Output and provide continuity to the overall explanation.

#### MULTIPLEX PROGRAM STEP (INITIAL CYCLE)

I—0 Time is a normal cycle. The PSAR is read and the MAL loaded to define the address of the next program step. The PSAR data is bumped by 2 and written back in the PSAR.

I—1 Time is a normal cycle. The Multiplex program step is read from the memory location defined by the MAL. The Multiplex program step is transferred to the A-Word, written back into its memory location and the Operational Code latches are loaded to define Multiplex Output Indirect.

I—2 Time is a normal output cycle except for setting the Multiplex latch. The A-Word (Program Step) data is read, the MAL is loaded and the A-Word is preserved. Y11 will be loaded during Bit 9/12 Time because the program step format will contain a bit in the 11th bit position to define Multiplex. The Y8, Y9 and Y10 outputs (all down) will define the Output Device by setting the Translator Select latch at I—2, Bit 9/12 Central

Bit Time. With Y11 on from Bit 9/12 Time, the Multiplex latch will set at Bit 13/16, Central Bit Time (remember, we are assuming the Translator is idle, i.e., ready during the first Output step).

I—3 Time is a normal Indirect Output cycle except Reset Y is turned on by Multiplex, Ready and I—3 Time. The MAL is reset to define the address of Register 0. Remember, in a Multiplex program step, Register 0 will always contain our Indirect Address data. Register 0 will be read and its address data transferred to the B-Word. Since this is an indirect address, the address data is bumped by 1 before being written back into Register 0.

I—4 Time is a normal Indirect Output cycle. The B-Word address data is read and the MAL loaded to define the Byte to be outputted. The B-Word is not rewritten and will be cleared.

I—5 Time is a normal Output cycle. The Byte to be outputted is read and transferred to the Output Latches during Bit 1/4 and Bit 5/8 Central Bit Times. The Current Source Y Logic signal will be down during Bit 9/12 and Bit 13/16 Time. Busy is set at I—5, Bit 13/16, Steer Latch Strobe Time by Not Halt, Output, Ready, Not Lights. Busy resets Ready, ANDS with Translator Select, Not Function and Not Output Interface Feedback to bring up Translator Print, and the Translator cycle clutch is energized. The Clock permutes to I—0 to begin the next program step. Keep in mind the CCU is much faster than the mechanical devices, therefore, the next program step is begun long before the Translator cycle clutch actually starts driving the mechanism.

#### COMPOSITION PROGRAM STEP CYCLES

At I—0, Begin Program Step Time, Ready will not be turned back on because Busy is still on — the Translator must cycle to approximately 65 degrees to turn off Busy. With Multiplex up and Ready down, normal CCU cycles will occur unless, as previously explained, an Output step is read.

During I—0 Time the PSAR is read and the MAL loaded to define the next program step address. The original PSAR address data is bumped by 2 and written back into the PSAR.

During I—1 Time the program step is transferred to the A-Word, preserved in memory and the Operational Code Latches are loaded to define the SCAT function.

I—2 through I—9 will depend on the SCAT function and will be normal CCU cycles. At the end of the last “I” Time the Clock will permute to I—0 and the next program step begins.

The Composition program steps will continue until the Translator is again ready to accept another character. Review “Translator Cycle” for contact and signal timing involved.

#### MULTIPLEX PROGRAM STEP (2ND CYCLE)

The Translator has outputted the first character to the Printer and is ready for another character. Busy is down and Output Interface Feedback\* is up. The CCU is still performing Compo-

sition program steps. When the Composition program step in progress completes its last "I" Time, the Clock will permute to I-0 Time to begin the next Composition step. This step must be interrupted and preserved as the CCU is forced into another Output step to output the second character.

At I-0, Begin Program Step Time, with Not Busy up and Not Output Interface\* up, Ready will be turned on. The PSAR is read and the MAL is loaded to define the address of the next Composition program step. The PSAR address data is bumped by 2 and written back into the PSAR. This is a normal I-0 cycle except for turning on Ready.

During I-1 Time the Composition program step is read, transferred to the A-Word and preserved in memory. The Operational Code Latches will not be loaded as usual. The Load Operational Code signal will be down because Multiplex and Ready are both on (Not Multiplex and Not Ready down). No Operational Code latches will be loaded from the P-Buffer outputs as the program step is transferred to the A-Word. However, the Upset Pre-Inhibit signal, which is up every I-1, Bit 13/16 Time, will AND with the Multiplex and Ready signals to set Operational Code 4 and Operational Code 6 to define "Indirect Output to Translator". With both Multiplex and Ready up, we have "forced" an Output step. Upset Pre-Inhibit, Multiplex and Ready will also set the Pre-Inhibit Latch as Output comes up.

At I-2 Time, Pre-Inhibit will set the Inhibit Latch. Inhibit will prevent the bump by 2 of the PSAR during the next I-0 Time and force an A-Word to A-Word Address during the next I-1 Time. Thus, the interrupted Composition program step will be preserved. The Inhibit function has been covered in detail previously. Other than setting Inhibit, the I-2 cycle is a normal cycle. The Composition program step (A-Word) is read during I-2 Time and the MAL loaded with the format address data. This is invalid data at the moment, however, because we always use Register 0 as our indirect address register during Multiplex. This situation will be handled during I-3 Time.

At I-3 Time, Multiplex and Ready will bring up the Reset Y signal. The MAL will be reset to clear the address data loaded in the previous I-2 Time. With the MAL reset (no Y's loaded), the MAL defines the address of Register 0 which always contains our indirect address data for Multiplex. Register 0 will be read and the Byte address data transferred to the B-Word. The original data is bumped by 1 and written back into Register 0.

During I-4 Time the B-Word is read and the MAL is loaded to define the Byte address from which the next character is to be outputted. The B-Word is not written back and will be cleared.

During I-5 Time, the Byte addressed by the MAL is read and transferred to the Output Latches during Bit 1/4 and Bit 5/8 Times. Current Source Y Logic will be down during Bit 9/12 and Bit 13/16 Times. At Bit 13/16 Steer Latch Strobe Time, Busy is set to start the Translator cycle. Busy also resets Ready to indicate the Translator is operating on a character. At the end of Bit 13/16 Time, the Clock permutes to I-0 and the next program step begins.

This program step will be the preserved Composition step which was interrupted by the forced output step. The CCU will continue performing Composition program steps until the Translator is ready for another character — at which time the Composition program step sequence is interrupted and preserved as another output step is forced.

This process will continue until a Byte is read at I-5 of the forced Output step, which contains all 8 bits on. This is a HALT code. When the Output Latches have been loaded with the Halt Code, Halt comes up to prevent turning on Busy to start the Translator. The Translator does not cycle and so no Printer action occurs. The Clock will permute to I-0 Time.

The Begin Program Step signal at I-0 turns Ready back on and resets the Multiplex Latch and the program step routine returns to normal. The Halt code will remain in the Output Latches until reset during the next Output program step.

## TRANSLATOR

### GENERAL

The Translator is an electro-mechanical device used to convert the CCU electronic signals to mechanical energy to operate the printer. It is mounted in the console desk and may be tilted up for service. The cable connections to the CCU are long enough to allow removing the Translator and placing it on the rear of the desk if necessary for maximum accessibility.

The printer may be raised and lowered on a spring loaded Printer Support Frame which mounts and pivots on two studs mounted in the rear of the Translator stationary frame (Fig. 1). The spring counter-balances the weight of the printer, allowing the printer and support frame to be raised and lowered by turning a knob located under the console desk. Positioning pins on the printer seat in locating contours, mounted on the front of the Translator frame, assuring the printer keylever links will be aligned with the Translator actuator links. In the operating position, the printer rests on three (3) adjustable support screws. One support screw is located in the back and one on either side at the front. An adjustable screw on each side of the printer bottom cover rests on the two front support screws. Individual adjustment of the support and cover screws allows compatibility between different printers on the same translator. As the printer is raised and lowered, the Translator actuator links are cammed backward and forward. This allows the actuator links and printer keylever links to be automatically disconnected or connected as the printer is raised or lowered.

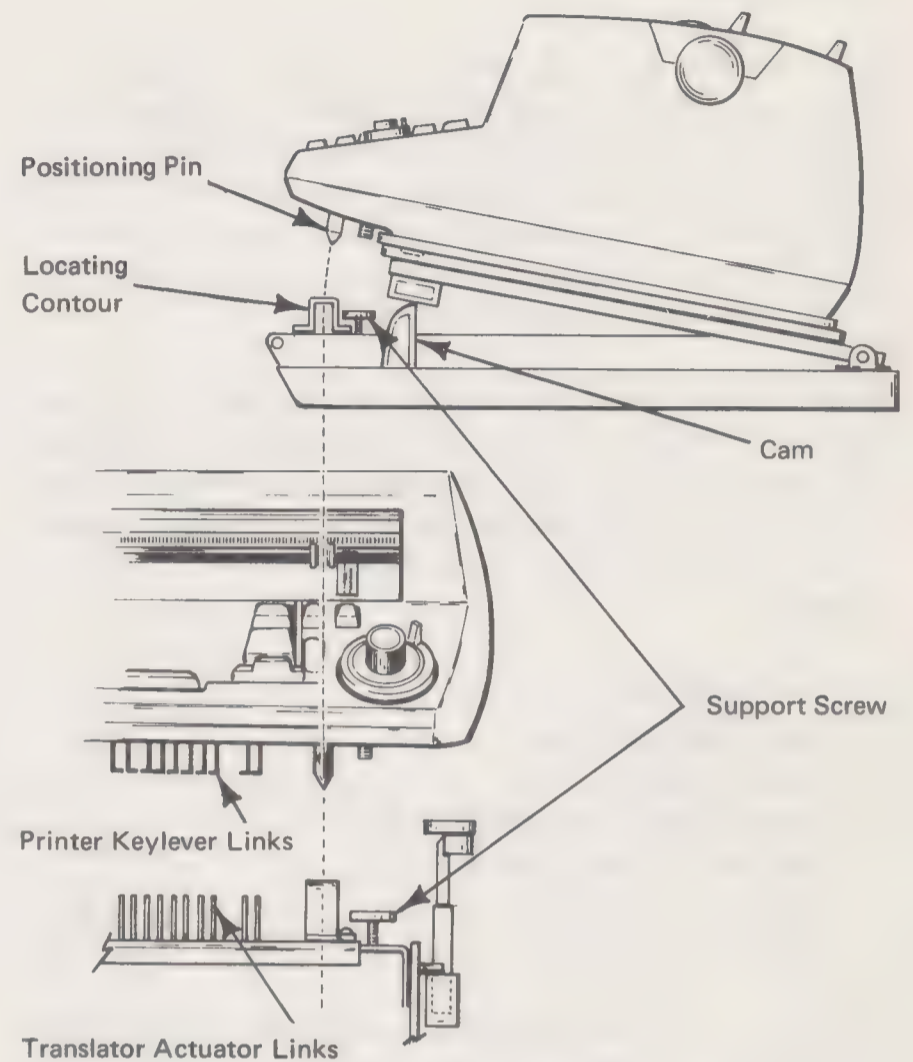


Figure 1

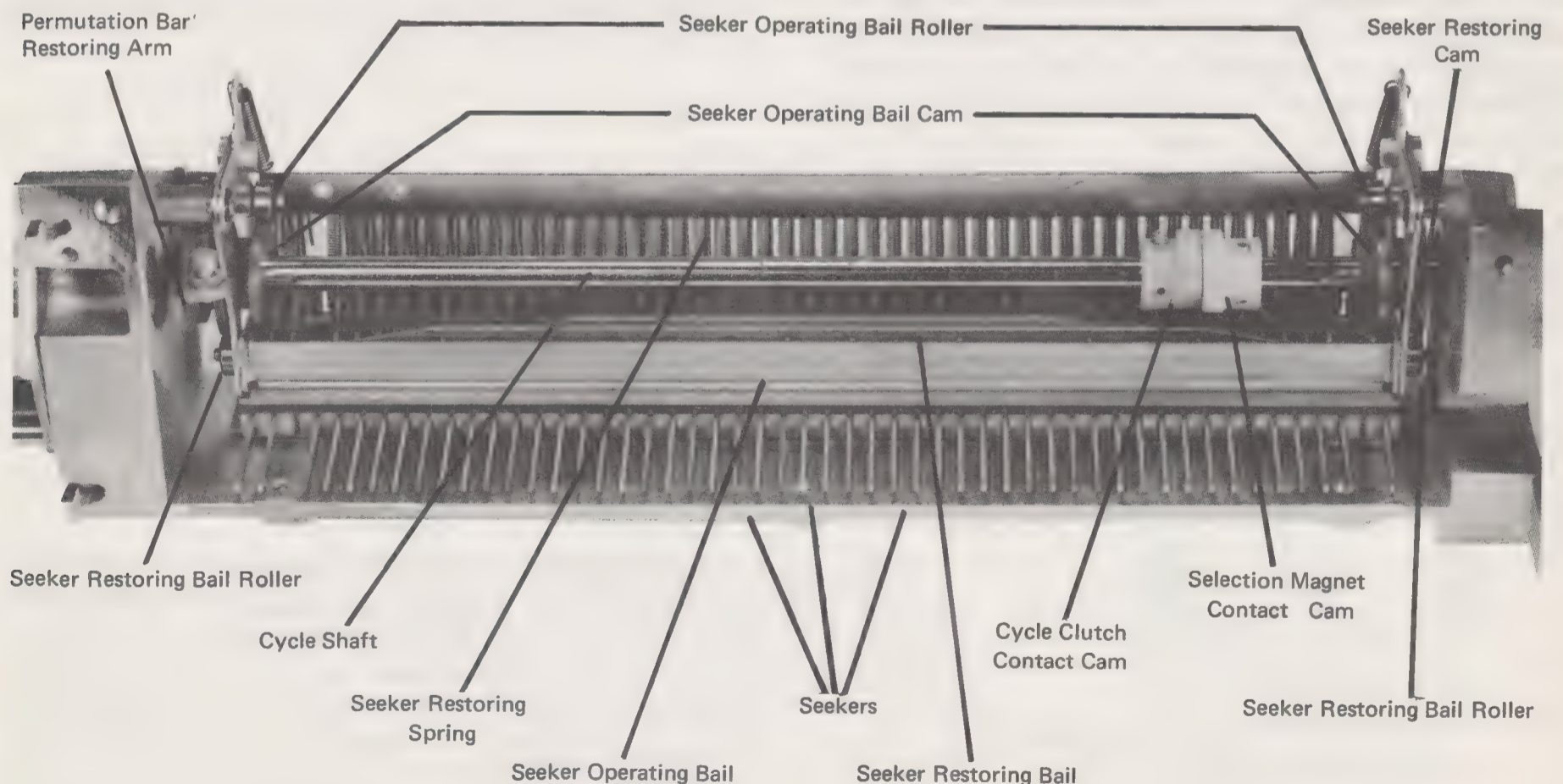


Figure 2

The electrical connections to the printer photo-cells are through a fourteen (14) position self-aligning plug which also couples and uncouples automatically. Line voltage for the printer motor is supplied through the standard printer line cord which plugs into a receptacle mounted on the Translator frame.

## OPERATION

Drive for the unit is supplied by a 1/35 h.p. motor which drives a spring clutch via a cog drive belt. The spring clutch is controlled by an armature, armature magnet assembly, and backlash detent. The spring clutch is similar to other spring clutches used on IBM equipment and will not be discussed in detail. When the armature is attracted, the spring clutch will drive the cycle shaft through 360 Deg.

The cycle shaft is mounted in two ball bearings, one on each side of the translator frame (Fig. 2). Five steel cams, keyed and set screwed to the cycle shaft, drive the restoring and operating bails. Two nylon cams, set screwed to the cycle shaft, operate the two feedback contacts. From right to left, the cams are designated:

1. Permutation bar restoring
2. Seeker restoring, right
3. Seeker operating, right
4. Cycle Clutch Contact (Nylon)
5. Selection Magnet Contact (Nylon)
6. Seeker operating, left
7. Seeker restoring, left

Two magnet packs, containing four (4) selection magnets each, control the seven (7) permutation bars. One magnet is not used, since only 7 bars are needed for MT/SC operation. These permutation bars have a lug which engages a notch in the selection magnet armatures (Fig. 3). The permutation bars are normally held to the left by the permutation bar restoring bail. In the rest position, the lugs clear the armature notch latching surface slightly to allow the armatures to operate freely when their respective magnets are energized. The magnets are numbered as shown in Figure 4.

During a normal cycle, the Translator cycle clutch and some combination of selection magnets will be energized by signals from the CCU. As the motor drives the cycle shaft, the permu-

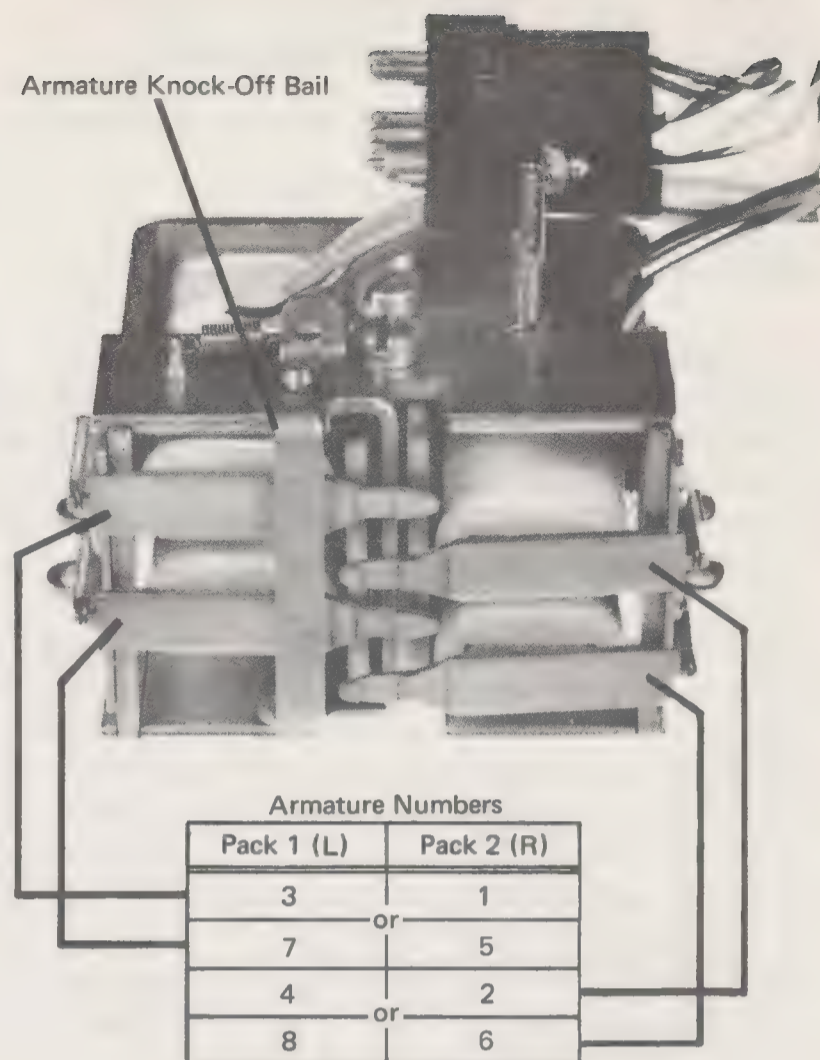
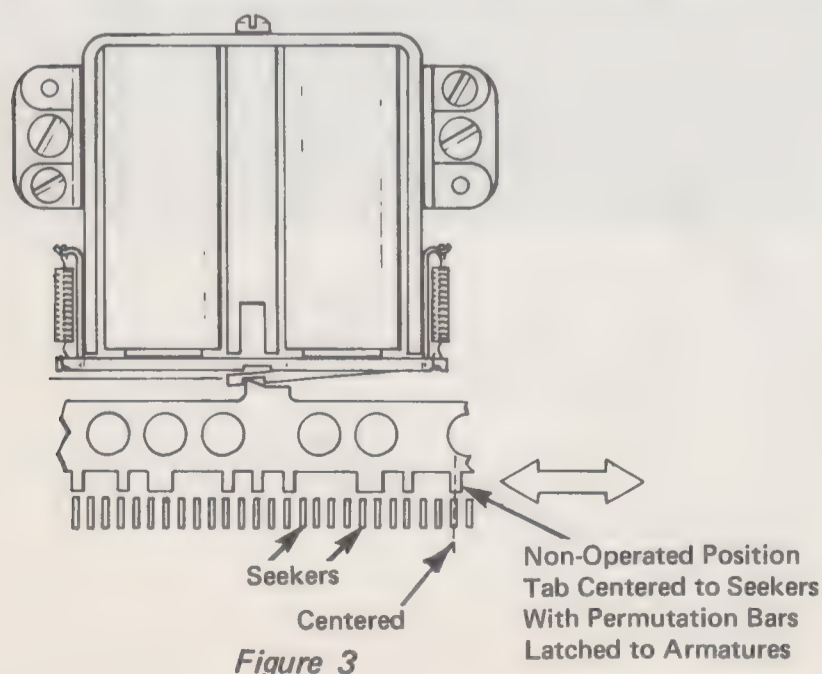


Figure 4

tation bar restoring bail moves to the right. The permutation bars, under spring tension, attempt to follow the restoring bail. If the armature associated with a permutation bar is attracted, the permutation bar will be allowed to move to the right to its "Operated Position" (Fig. 5). If the associated armature is not attracted, the lug on the permutation bar will engage the notch in the armature and the permutation bar will be stopped in the "home position".

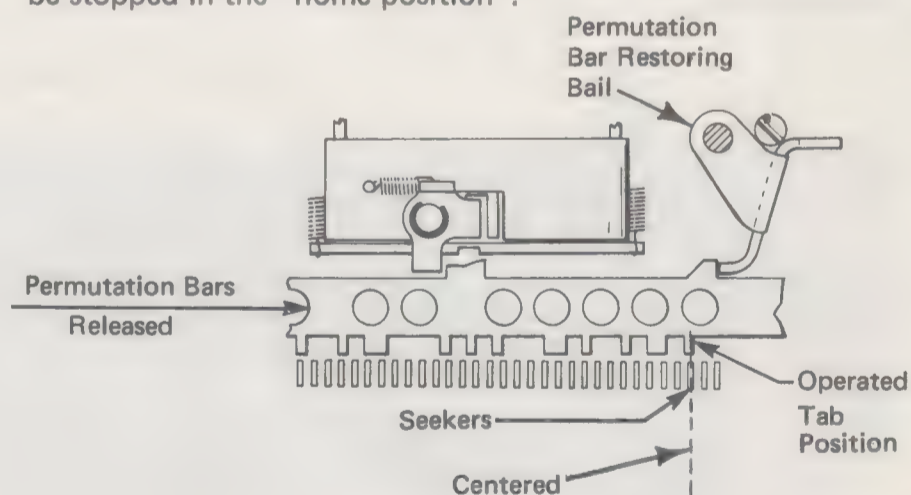


Figure 5

Each permutation bar contains 104 projections. The odd numbered projections are called the "home position projections" while the even numbered projections are called "operated position projections". These projections are on the lower side of the permutation bar. A code for each character and function is obtained by removing some of the projections from each bar. As the permutation bars shift to the "home" and "operated" positions, the projections will be aligned on the seven (7) bars so that there is at least one projection above every seeker, except in the row above a desired seeker.

The seekers are operated by the seeker operating bail and supply motion to the actuating links. The seekers are mounted in a "U" shaped guide comb which is a part of the frame unit. The front end of the seekers are held down in the front guide comb by a fulcrum rod. The rear end of the seekers ride in the rear guide comb with lateral support only. An extension spring on each seeker loads the seeker forward against the front guide comb fulcrum rod and up against the seeker restoring bail at the rear (Fig. 6). The seeker operation bails' rest position is toward the rear (Fig. 6). It is cam driven forward past the notch in the seekers during the initial part of the cycle (Fig. 7).

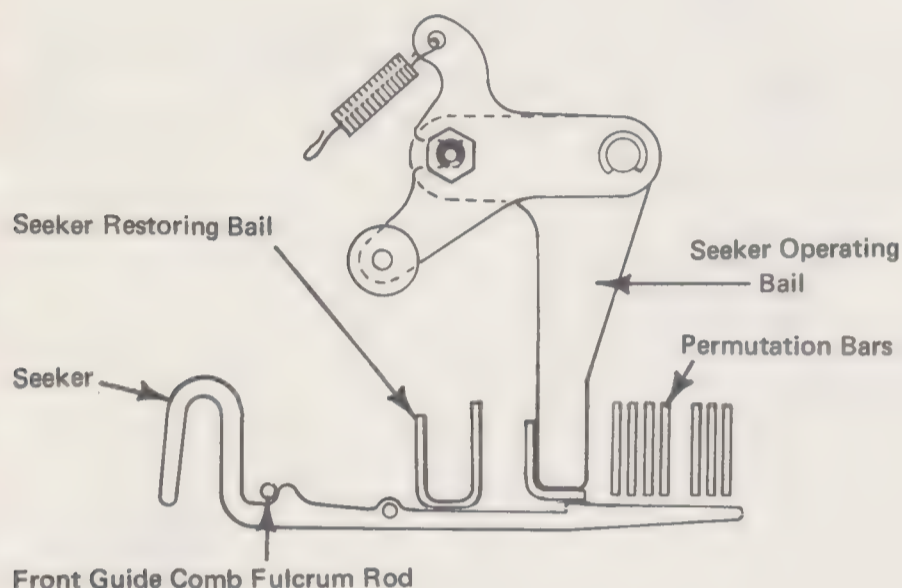


Figure 6

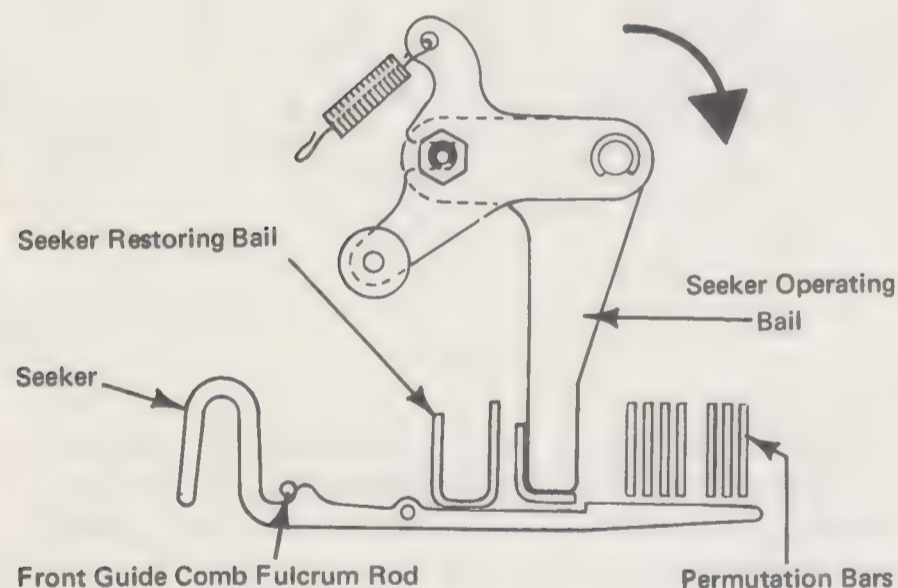


Figure 7

As the seeker restoring bail moves upward during the cycle, the rear end of the seekers will follow under their spring tension. As the seeker restoring bail continues to rise, the seeker below the permutation bar row which has all the projections removed will rise to its active position (Fig. 8). All the other seekers will be stopped by the projections on the permutation bars.

Normally, only one seeker will be allowed to rise to the active position. However, in a no-print cycle, the no-print seeker will also reach the active position. With the seeker in its active position, the rear step on the seeker will be in position to overlap the seeker operating bail (Fig. 8).

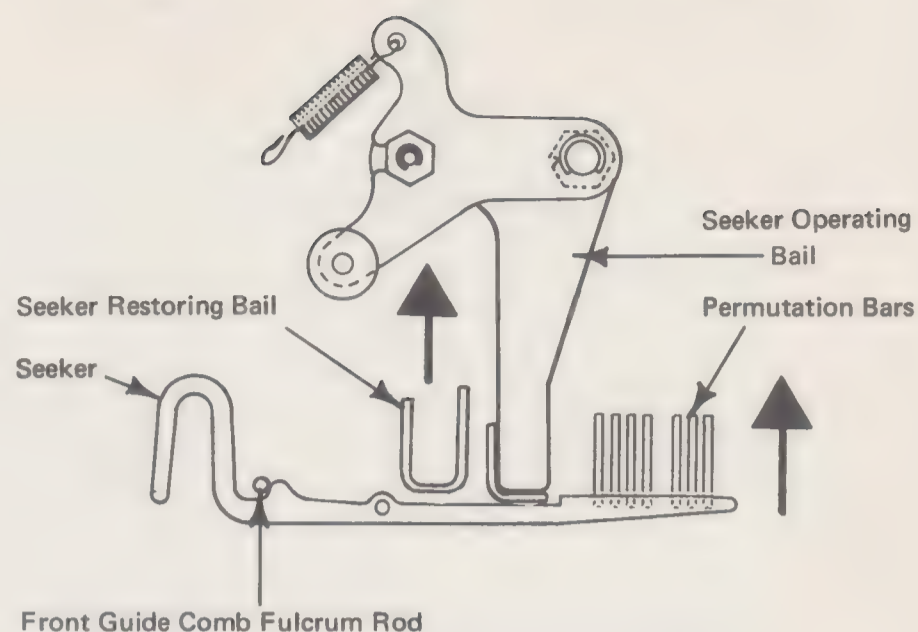


Figure 8

The seeker operating bail moves toward the rear under spring tension as its cam follower rollers move toward the low dwell of the seeker operating bail cams (Fig. 9). The active seeker is pulled toward the rear by the operating bail and produces a pull on its associated actuator link.

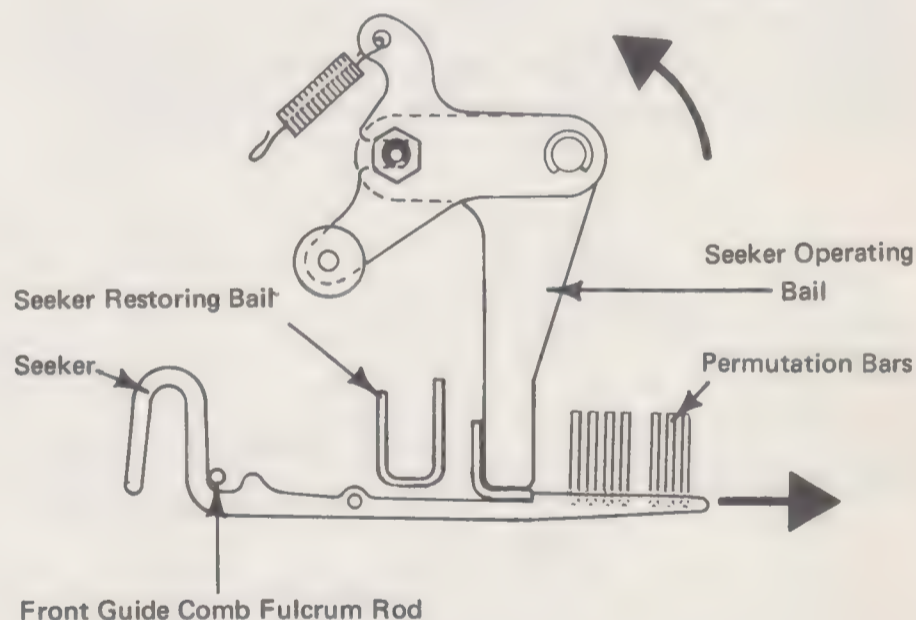


Figure 9

The actuator links transmit the seeker motion to the printer keylever links (Fig. 10). The actuator links are mounted above the seekers in a guide comb and pivot on a fulcrum rod which runs through the guide comb. A second guide comb mounted across the top of the main frame supports the upper end of the actuator links just below the point where they make contact with the keylever links. Each actuator link is spring loaded with an extension spring near the bottom. This loads the bottom of the actuator links toward the front so they remain in contact with the "hook" surface of the seekers.

As the seeker operating bail moves toward the rear, the rearward pull on the actuator causes it to rotate and produce a downward pull on the keylever link.

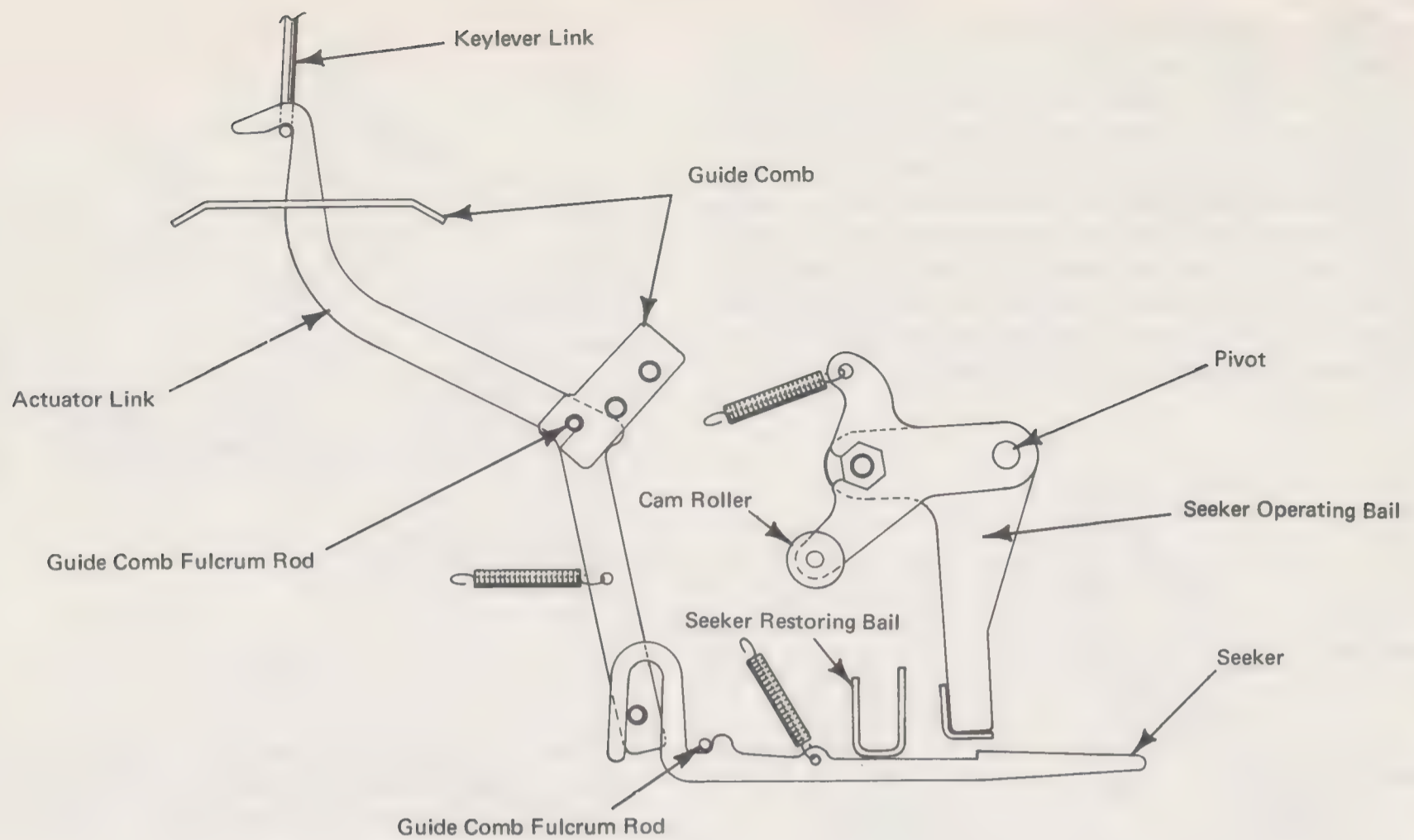


Figure 10

The seeker restoring bail is driven downward as its cam rollers ride up the high lobe of the cams. The active seeker is disengaged from the operating bail and restores forward under spring tension (Fig. 11). Continued movement of the restoring bail moves all the seekers away from the permutation bar projections.

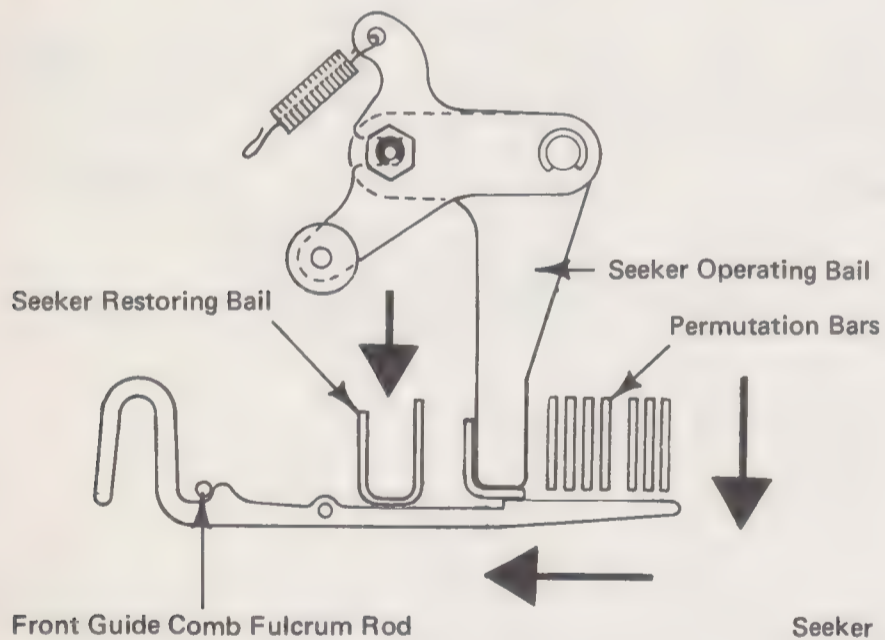


Figure 11

The permutation bars are restored near the end of the cycle. The permutation bar restoring cam drives the permutation bar restoring arm cam follower roller upward causing the restoring arm to rotate downward at the rear. The adjusting screw in the restoring arm pushes down on the restoring bail causing it to rotate clockwise. The lower edge of the restoring bail engages the restoring lugs on the permutation bars and moves them to the left (Fig. 12). As the latching surface of the permutation bars move past the armature notches, another projection on the permutation bar will contact the armature knock-off bail. The

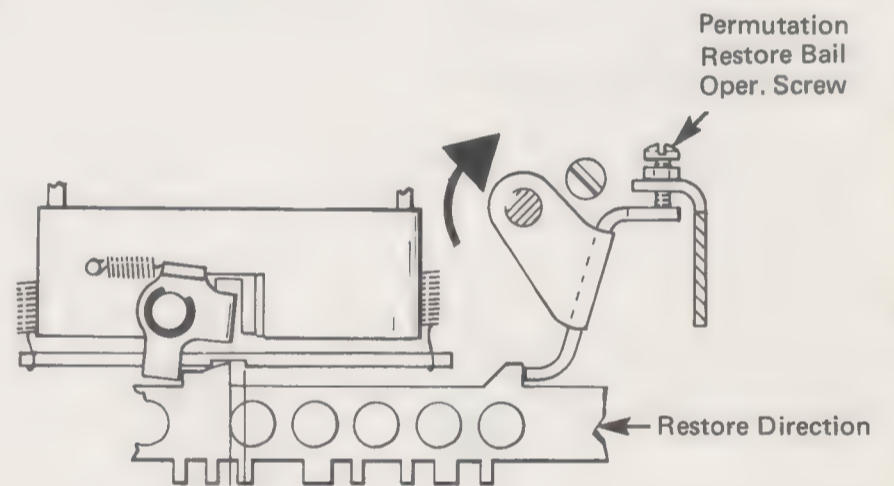


Figure 12

bail rotates clockwise and forces the armatures away from the cores to overcome any residual magnetism (Fig. 13). The armatures are now in position to allow the non-selected permutation bars to engage the latch surface on the next cycle.

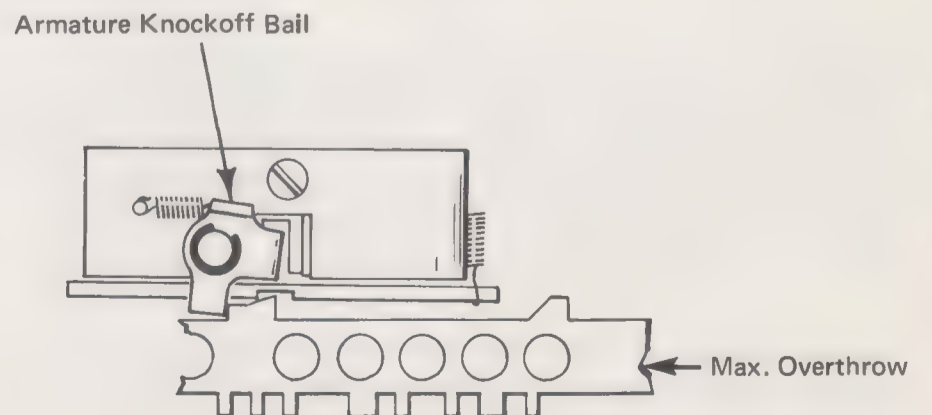


Figure 13

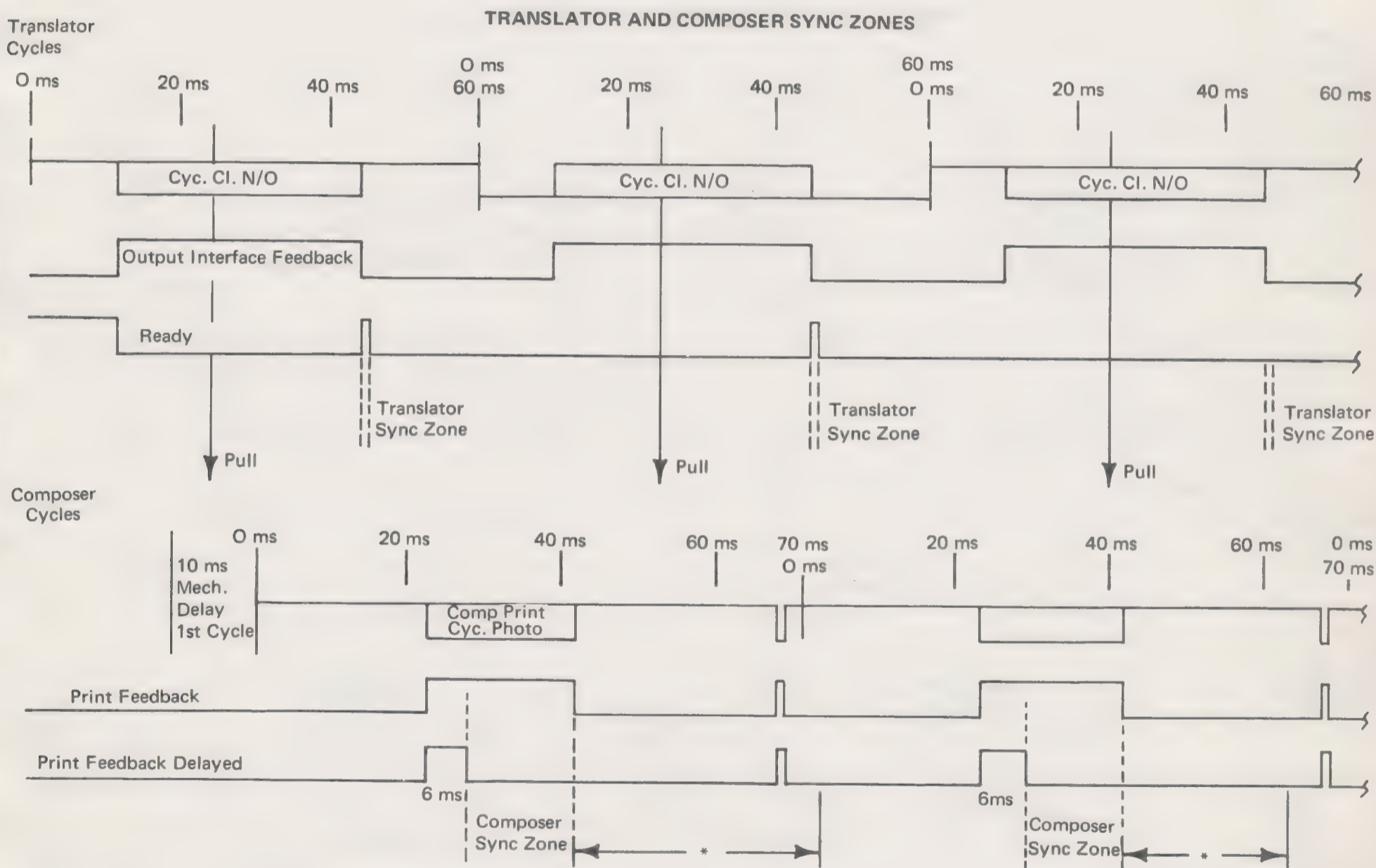
## SYNCHRONIZATION

Maximum output of camera ready copy can only be achieved by operating the output device at maximum speed. Because of the inherent speed differences of motors due to line voltage, age, varying loads and initial manufacturing tolerances, etc., it is necessary that the Translator speed be greater than the printer speed under all circumstances. Therefore, because there is a definite speed differential between the two units, and because there is a restricted zone in which a keylever may be pulled, some sort of synchronization is necessary to keep the two units in step.

There are requirements, also, demanded by the printer, that certain functions be preceded by a time interval to allow the printer to completely restore its mechanical latches.

## Ordinary Synchronization

The synchronization required simply because of the speed differential between the units, is referred to as Ordinary Synchronization. If one observes the action of the Translator with the printer as a reference, the Translator motion appears to regress, or back into, the printer. If the printer point of reference is the cycle shaft photoelectric "window", and the Translator cycle clutch contact is observed, the leading edge of the cycle clutch N/C contact appears to "back into" the trailing edge of the "window" (Fig. 14). When these two points overlap, then the next keylever pull would be in the non-permissible pull zone of the printer. Therefore, it is necessary to temporarily halt the Translator.



NOTE: Translator and Composer cycle times for illustration only. In reality the Translator runs only slightly faster than the Composer.

\* Time that the Composer must loose before synchronization

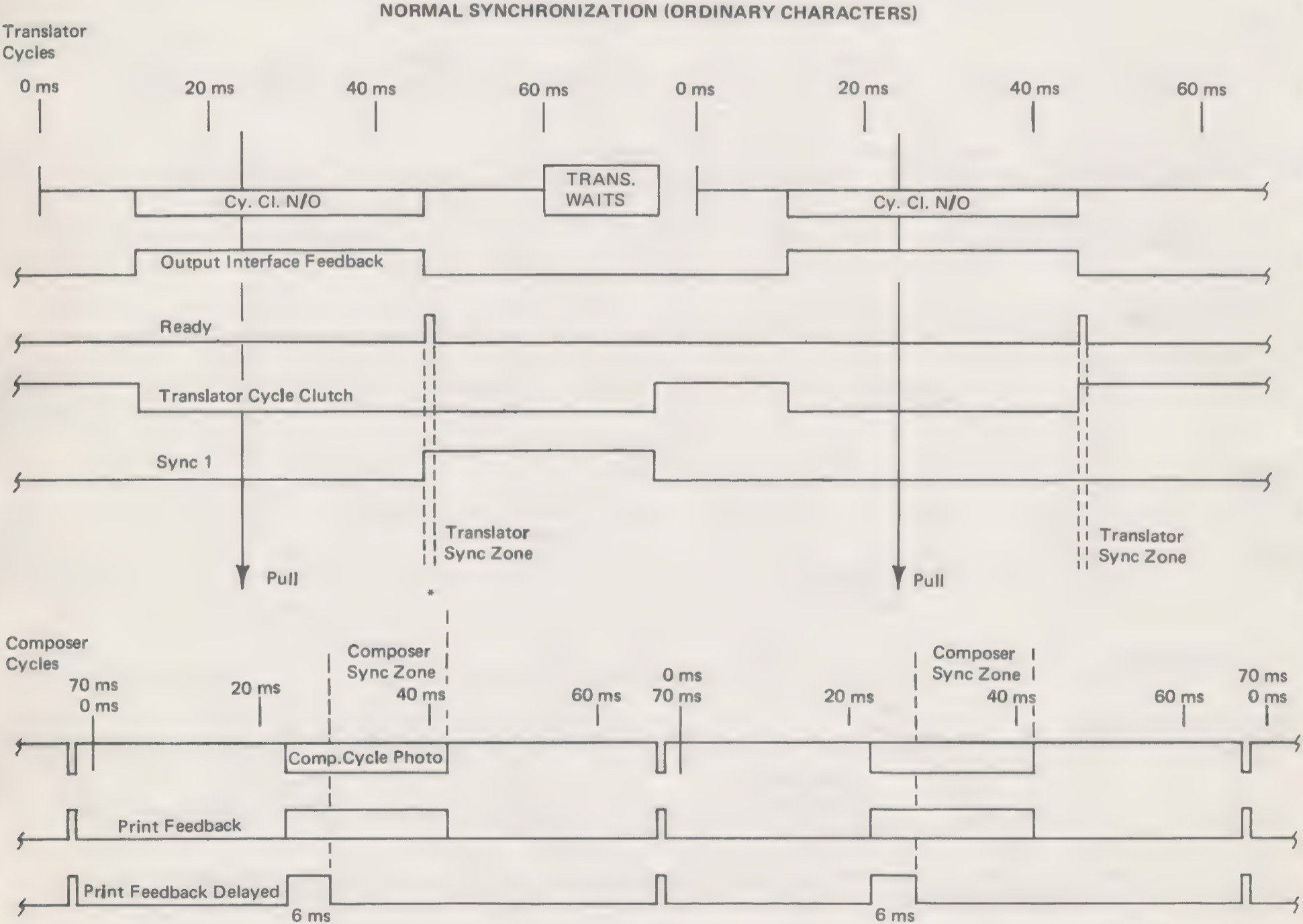
Figure 14

The two points mentioned, when overlapped, cause the SYNC 1 latch to be set (Fig. 15). The cycle clutch N/C contact will make at 280 Deg. of the Translator cycle. The cycle clutch N/C signal is ANDED with the NOT DUMMY and NOT TAB or CARRIER RETURN signals to reset Output Interface Feedback which resets Output Interface Feedback\*. At Begin Program Step time, Ready is turned on to indicate the Translator is ready to accept the next character. This is the standard "Ready-Busy" logic covered in the section on Output to Translator. However, if the Printer "window contact" is made, the Printer Feedback signal will be up, indicating that the Printer is NOT ready for another character. Ready was turned on at I-0, Begin Program Step time. At I-1, Bit 13/16 time, Upset Pre-Inhibit will come on. Upset Pre-Inhibit, Ready and Print Feedback will set Sync 1 if the character in the Output Latches is an Ordinary Character. The NOT Sync signal goes down and prevents picking the Translator cycle clutch as long as the Sync 1 latch is set. The narrow slot in the printer cycle shaft "contact" occurs at approximately 170 degrees of the printer cy-

cle. This signal is used to reset the Sync 1 latch and free the output logic. The Translator cycle clutch is energized again, and the next keylever pull will occur just before the end of the printer's permissible zone. Thus, the Translator will run the maximum number of cycles before another synchronization is necessary.

Ordinary Synchronization can only take place for ordinary characters, that is, non-function characters, since only ordinary characters cause the printer cycle shaft to rotate. Consequently, any time a function is encountered, the ordinary sync is rendered inoperative.

Any function code causes a sequence of electronic circuits to "time out" two Translator cycles. What actually happens during these two cycles varies between functions, but the sequence itself always occurs. The various functions under consideration are shift, unshift, backspace, tabulation, and carrier return.



NOTE: Translator and Composer cycle times for illustration only. In reality the Translator runs only slightly faster than the Composer.

\*The Translator sync zone moves into the Composer sync zone. Sync 1 latch sets and will remain set until the Composer nears the end of its cycle (170 Deg. to 175 Deg.). The short printer feedback signal near the end of the Composer cycle resets Sync 1 and the Translator cycle clutch is picked again. The Translator sync zone and the Composer sync zone are now separated by some amount of time that is dependent upon the individual machines.

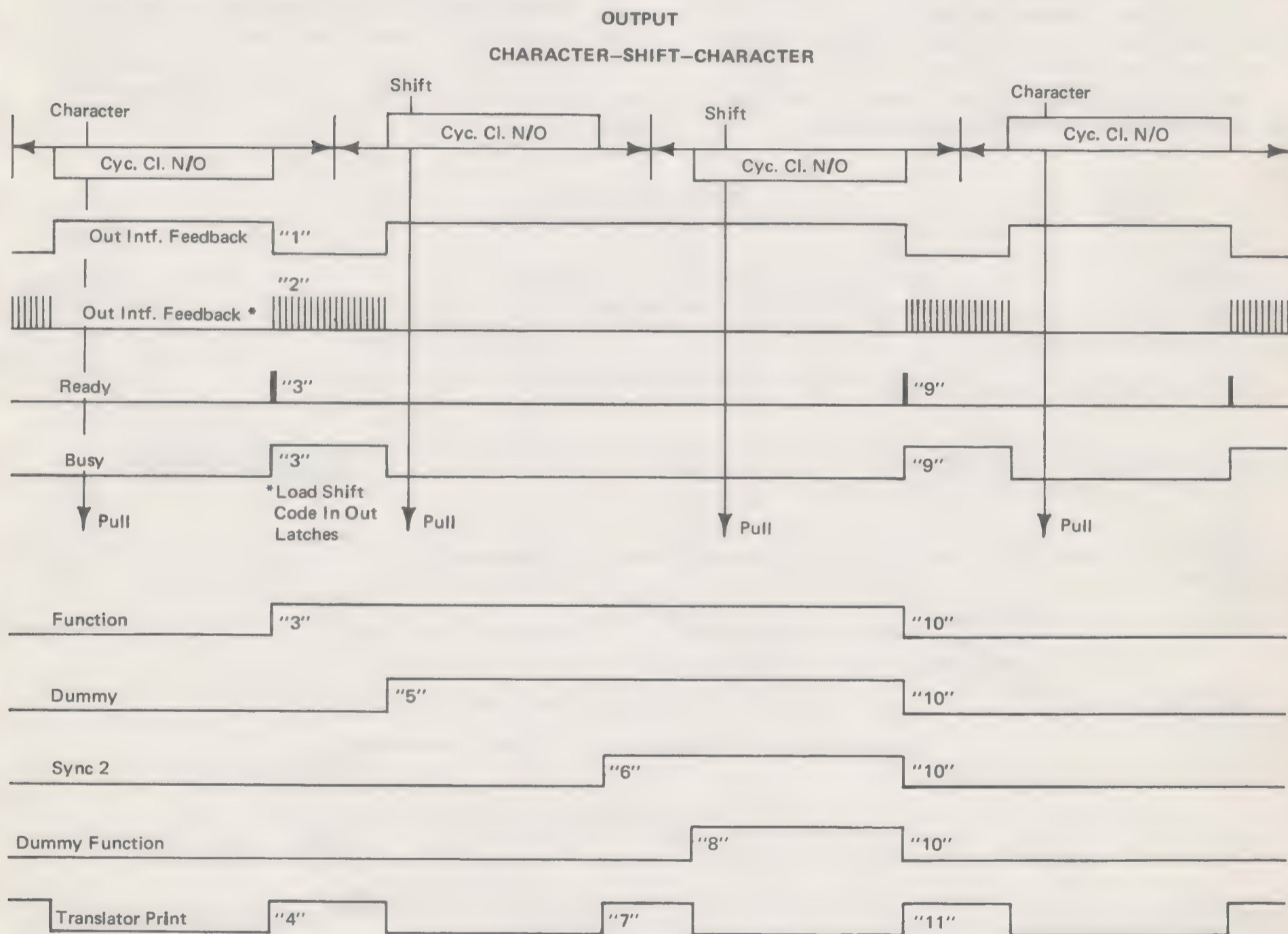
Figure 15

## Shift and Unshift Synchronization (Normal Output)

Refer to Figure 16 for the character, shift, character sequence during a normal output. Output Interface Feedback will reset when the Cycle Clutch N/C contact makes at 280 degrees. Not Output Interface Feedback will reset Output Interface Feedback\*, so Ready can be turned on at the next Begin Program Step time. Assuming the next program step to be an Output step (shift to printer), the Output Latches will be loaded at 1-5 Time with the shift code. An upper case code will load Output Latches 1, 3, and 6, while a lower case code will load Output Latches 1, 3, 4, and 6. Translator Select will be up from 1-2 Time of this step, identifying the Translator as the

Output device. Translator Select is ANDED with Output Latch 6 and Not Output Latch 2 to turn on Function. When Busy comes up at 1-5 Time, it will AND with Function and Output Latch 3 to turn on Translator Print and a shift code is sent to the printer. When Cycle Clutch N/O makes at 65 degrees, Output Interface Feedback is set as usual. However, with Function up, Dummy will also set when Cycle Clutch N/O makes.

At 280 degrees, Cycle Clutch N/C will make but will not reset Output Interface Feedback as usual because Dummy is set (Not Dummy down). With Cycle Clutch N/C and Output Interface Feedback both up, Sync 2 will set. Dummy, Not Dummy Function and Cycle Clutch N/C will turn on Translator Print



\*Shift Code = U.C.-Out 1, Out 3, Out 6      L.C.-Out 1, Out 3, Out 4, Out 6

Figure 16

again and a second shift code will be sent to the printer. The Output Latches still contain our shift code because the Load and Reset Output Latch signals cannot turn on until Ready is set, and Ready cannot be set as long as Output Interface Feedback is up..

When Cycle Clutch N/O makes at 65 degrees of this second cycle, Dummy Function will set because Sync 2 and Dummy are set. Dummy Function will set up the reset of Output Interface Feedback.

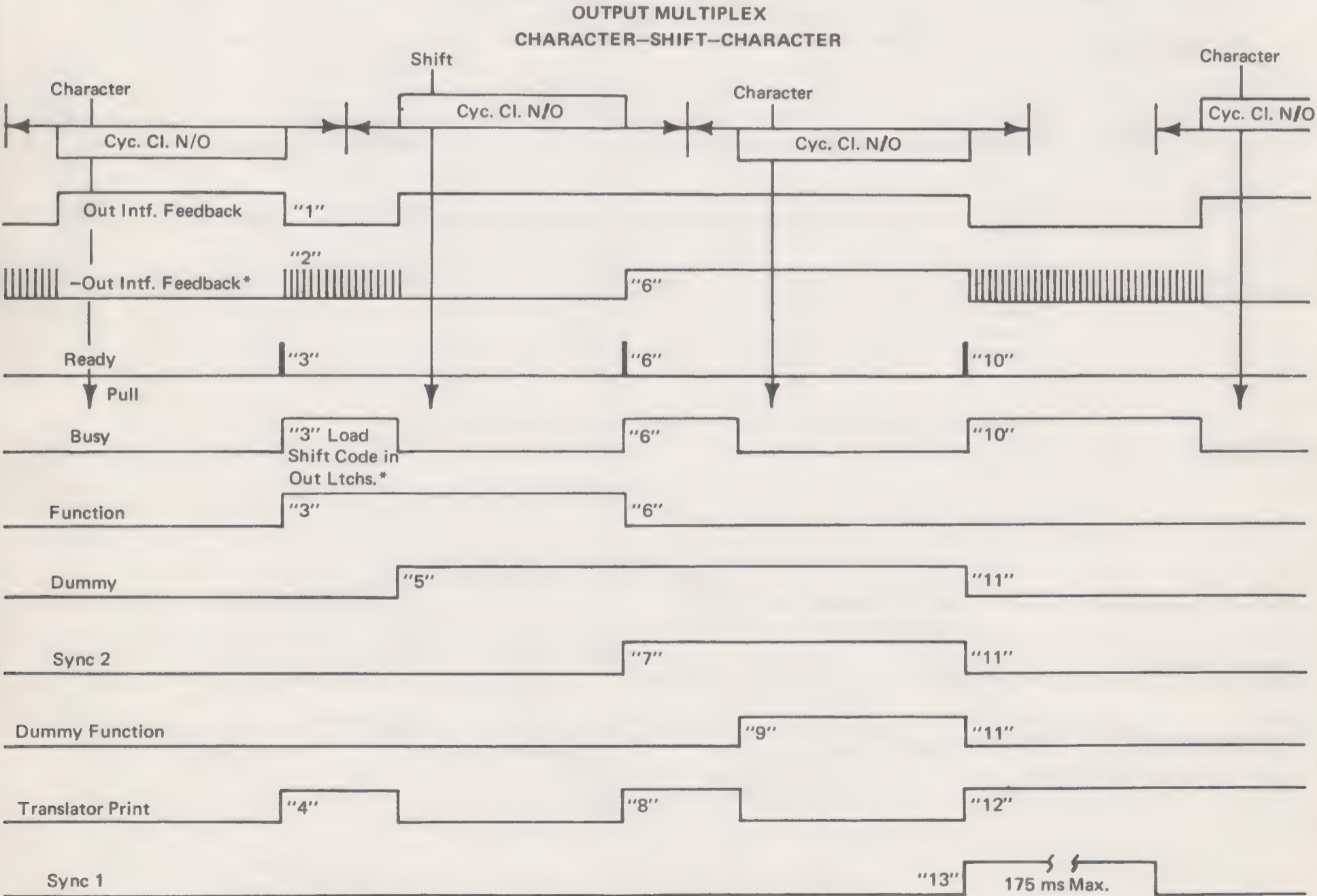
When Cycle Clutch N/C makes at 280 degrees, Dummy Function, Not Carrier Return Interlock and Not Tab or Carrier Return Single Shot will reset Output Interface Feedback, which resets Output Interface Feedback\*, Dummy and Sync 2.

With Output Interface Feedback\* down, Ready will be set at the next I-0, Begin Program Step time and the program sequence will continue. At I-1 time, Upset Pre-Inhibit will come up, AND with Ready and reset Dummy Function. Function will remain on until a character code is loaded in the Output Latches at I-5 Time of the next Output program step.

### Shift and Unshift Synchronization (Multiplex)

During a Multiplex Output, the shift or unshift keylever will be operated during the first Translator cycle, and the character keylever pulled during the next cycle. This character will be stored in the printer keyboard (shift interlock) and the Sync 2 Latch set. Further output is inhibited until the printer cycles to print the character.

Refer to Figure 17 for the character, shift, character sequence during a Multiplex Output step. Output Interface Feedback will be reset by Cycle Clutch N/C at 280 degrees of the first cycle and will reset Output Interface Feedback\*. Ready will turn on at the next I-0, Begin Program Step time. At I-5 time of the Output step (shift), the Output Latches are loaded with the shift code. Lower case shift will load Output Latches 1, 3, 4, and 6, while upper case shift will load Output Latches 1, 3, and 6. Translator Select is ANDED with Output 6, Not Output 2 to turn on Function. When Busy is set at I-5, Bit 13/16 time, Translator Print will come up to pick the Translator cycle clutch and selection magnets to send the shift code to the printer.



\*Shift Code = UC-Out 1, Out 3, and Out 6 L.C.-Out 1, Out 3, Out 4, and Out 6

Figure 17

When Cycle Clutch N/O makes at 65 degrees, Output Interface Feedback is set as usual and Dummy will set because Function is up. Cycle Clutch N/C will make at 280 degrees and set Sync 2. Sync 2, Multiplex, Output Latch 3 and Function will reset Output Interface Feedback\* so Ready can be set at the next I-0 Time. With Ready on, another Output step is performed because we are in a Multiplex operation. At I-5 Time of this Output step we will assume a character is loaded in the Output Latches. This means the Function signal will turn off. Dummy, Not Dummy Function and Cycle Clutch N/C will turn on Translator Print to pick the cycle clutch and selection magnets in the Translator to send the character to the printer.

Dummy Function will set when Cycle Clutch N/O makes at 65 degrees of this cycle because Sync 2 and Dummy are set. At 280 degrees Cycle Clutch N/C makes and Output Interface Feedback is reset by Cycle Clutch N/C, Dummy Function, Not Tab or Carrier Return SS and Not Carrier Return Interlock. Resetting Output Interface Feedback causes Output Interface Feedback\* to be reset, thus conditioning Ready to be set at the next I-0 Time. Not Output Interface Feedback also resets Sync 2 and Dummy. Dummy Function, Not Function and Not Output Interface Feedback will set Sync 1.

Ready can now be turned on at the next BPS Time and the next Multiplex step initiated. Dummy Function is reset at I-1 Time by Upset Pre-Inhibit and Ready. Translator Print will be turned on by normal Busy logic at I-5 Time. With Sync 1 on,

the Translator cycle clutch will not be picked until the printer finishes the previous character (one following shift) and the Print Feedback signal resets Sync 1. Thus, the printer is allowed as much time as necessary to complete the shift operation and print the character following the shift.

### Backspace Synchronization

During a backspace function a dummy cycle occurs first and then the backspace keylever is pulled during the second cycle (Fig. 18).

When Ready is set following the character operation the backspace output step is initiated. At I-2 Time Translator Select will come on as usual to identify the Output Device. At I-5 Time, the Output Latches will be loaded with the backspace code (Output 1, 4, and 6). Function will turn on from the Output 6, Not Output 2 combination. At Bit 13/16 Time, Busy will be set. Busy, Function, Translator Select and Not Output Interface Feedback will turn on Translator Cycle Clutch since Sync 1 is down. The Translator will cycle but no Selection Magnets are energized because Translator Print is not on. This is our dummy cycle.

At 65 degrees, Cycle Clutch N/O will make to set Output Interface Feedback and Dummy. Dummy will prevent resetting Output Interface Feedback when Cycle Clutch N/C makes.

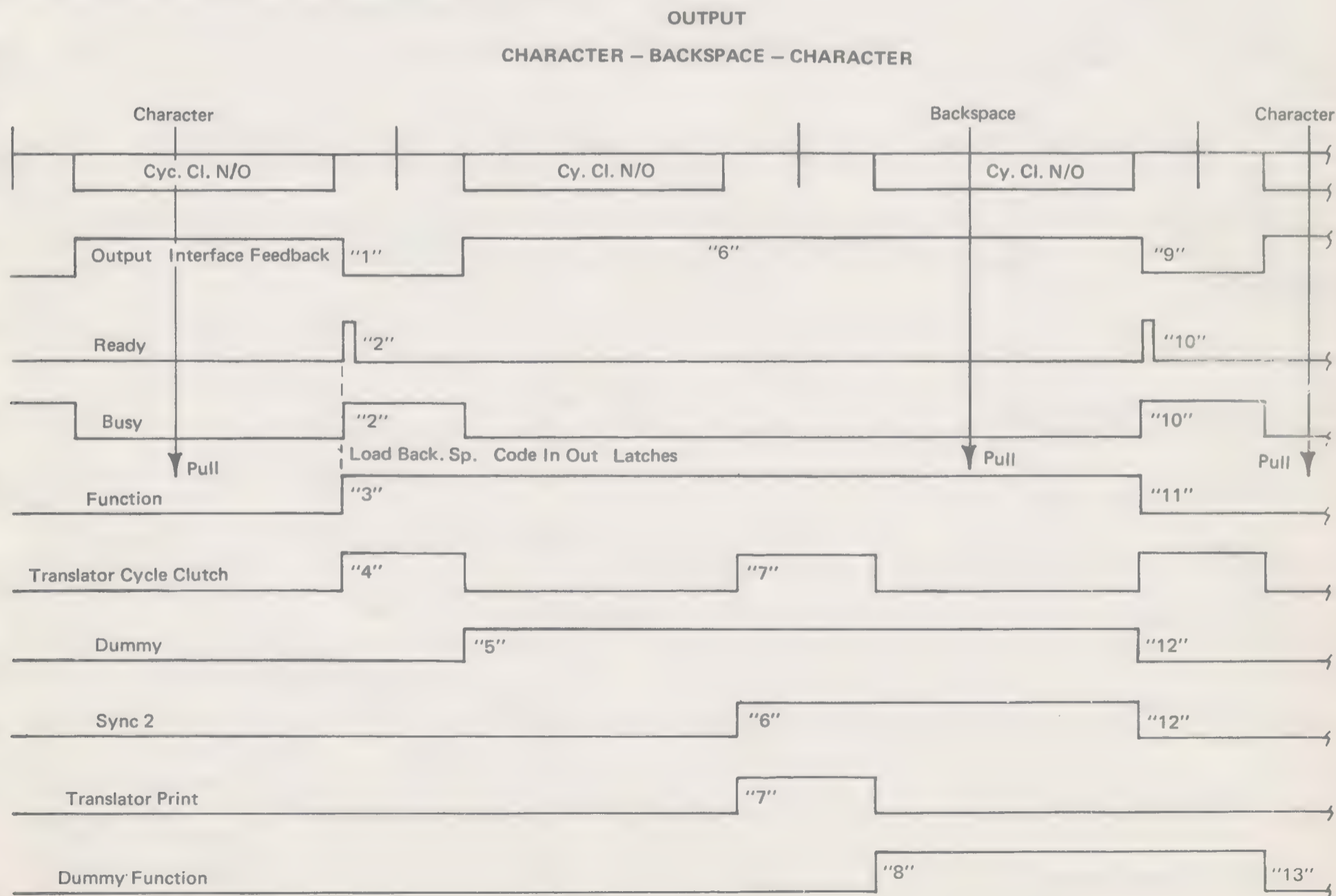


Figure 18

Cycle Clutch N/C will make at 280 degrees and set Sync 2. Also Dummy, Not Dummy Function and Cycle Clutch N/C will turn on Translator Print to repick the Translator Cycle Clutch and pick the Selection Magnets corresponding to our backspace code in the Output Latches. Thus, the backspace code is sent to the printer keylever.

When Cycle Clutch N/O makes at 65 degrees of this cycle, Dummy Function will set because Dummy and Sync 2 are both set. Dummy Function will cause Output Interface Feedback to be reset at 280 degrees when Cycle Clutch N/C makes (Dummy Function, CC N/C, Not Tab or Carrier Return SS and Not Carrier Return Interlock). Not Output Interface Feedback resets Output Interface Feedback\*, Sync 2 and Dummy.

At I-0 (BPS) Time, Ready will be set and another output step begun. At I-1 Time, Upset Pre-Inhibit will reset Dummy Function with Ready set. At I-5 Time of this step a character loaded in the Output Latches turns off Function and our Ready-Busy logic is back to normal.

CARRIER RETURN OR TAB SYNCHRONIZATION

On each of these functions, use is made of a second photoelectric device operated by the printer escapement shaft. The output of this "chopper wheel" is gated by a Tab or Carrier Return signal so it is inactive unless a tab or carrier return code is in the Output Latches.

On each of these functions, a dummy cycle occurs first, and the function keylever is pulled in the next cycle (Fig. 19). Just before the end of the second cycle, a timed delay called Tab or Carrier Return Single Shot is activated. Effectively, this single shot allows the printer carrier to begin moving to activate the "chopper wheel". The output from the "chopper wheel" is not used until the single shot has timed out. Thus, the presence of the "chopper wheel" signal after the single shot times out indicates the carrier is still moving. The output logic is inhibited by both signals; however, in the case of a short tab or carrier return, only the single shot signal will be needed since all carrier movement will have stopped by the time the single shot is over.

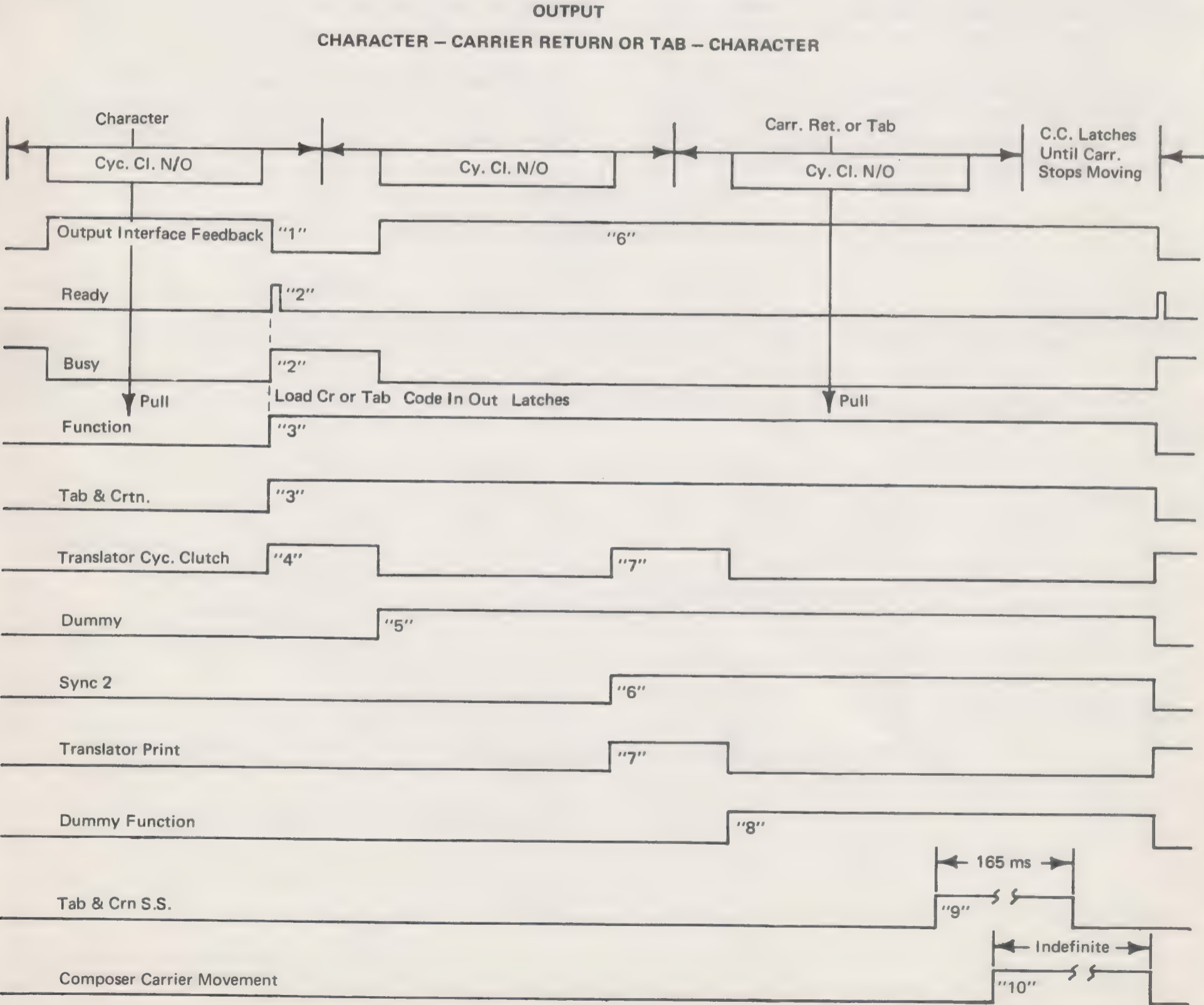


Figure 19

With Ready set at I—0, Begin Program Step time, the Output carrier return or tab step is initiated. The Output Latches are loaded with the tab or carrier return code at I—5 time. A carrier return will load Output 6 while a tab will load Output 4 and 6. Translator Select, Output 6, Not Output 2, will turn on Function and Tab + Carrier Return. When Busy sets at Bit 13/16 Time, the Translator Cycle Clutch signal will pick the Translator cycle clutch. The Selection Magnets are not energized because Translator Print is off. The Translator begins the dummy cycle.

At 65 degrees, Cycle Clutch N/O will make. Output Interface Feedback and Dummy will set.

Cycle Clutch N/C will make at 280 degrees to turn on Translator Print because Dummy and Not Dummy Function are up. The Selection Magnets are energized (C.R. or Tab code) and the cycle clutch is picked for the second cycle. Output Interface Feedback is not reset because Dummy is up; therefore, Sync 2 will set when CC N/C makes.

When Cycle Clutch N/O makes at 65 degrees of this second cycle, Dummy Function will set since Sync 2 and Dummy are

both set. With Tab + Carrier Return and Dummy Function both up, Tab + Carrier Return Single Shot becomes active for 165 ms when Cycle Clutch N/C makes at 280 degrees and prevents resetting Output Interface Feedback. As long as Output Interface Feedback stays on, Output Interface Feedback\*, Sync 2 or Dummy cannot be reset. This also means that Ready cannot be set to start another Output Step.

The carrier is now moving (either tab or carrier return) and the Carrier Return Interlock signal is up. Note that this signal also prevents resetting Output Interface Feedback. Therefore, the Ready logic will not be true until the single shot has timed out and the carrier movement is complete.

After the single shot times out and the Carrier Return Interlock signal goes down ("chopper wheel" inactive), Output Interface Feedback will be reset. This resets Sync 2, Dummy and Output Interface Feedback\* to free the Output logic. Dummy Function will reset during I—1 Time when Upset Pre-Inhibit comes up after Ready is set. Function and Tab + Carrier Return will turn off at I—5 Time of the next output step when a character is loaded in the Output Latches.



## PAPER TAPE READER

### INTRODUCTION

The IBM 6354 Paper Tape Reader is a modified version of the IBM 1054 Reader. It is designed to read 6 or 8 channel, advanced feel hole, chad type tape. The coding must be punched to Graphics Industry Standards.

When an Input from PT Reader program step is read, the PT Reader cycle clutch will be energized. Early in the cycle sensing fingers rise against the tape. If a hole is located above a sense finger, the sensing finger will pass through the tape and close an associated permissive-make contact. These contacts serve as inputs to an interface which adapts the PT codes to the normal CCU input interface. The character is stored in Memory through the P-Buffer just like the MT characters. After the character is read, the sense fingers move down and the tape is stepped to the next character. The cycle clutch is repicked for each character until an Elevate Code (carrier return) is read. The cycle clutch is not repicked and the inputted characters are operated upon as dictated by the program.

The PT Reader consists of four (4) basic mechanical units:

1. Motor and Drive
2. Cycle Clutch
3. Sensing Unit
4. Stepping Mechanism

### DRIVE

The drive is supplied by a shaded-pole motor. The motor drives a centrifugal clutch, which ensures that the motor can start under a heavy load. After the motor approaches normal operating speed, the clutch engages to drive the machine. The momentum developed by the motor starts the machine even though the cycle clutch may have been tripped.

### CYCLE CLUTCH

The cycle clutch pulley is mounted to a hub supported by a porous bronze bearing. The hub is in continuous rotation with the pulley whenever the motor is running.

A spring clutch forms the drive connection between the cycle shaft and the hub (Fig. 1). The right end of the clutch spring fits around the output hub on the cycle shaft. It is clamped to this hub by the clutch collar that encloses the right end of the spring. The tip of the spring is turned up so it fits into a gap in the collar. This arrangement prevents any slippage of the right end of the clutch spring, and makes it possible to adjust the position of the spring in relation to the shaft. The left end of the clutch spring fits around a shoulder on the input hub. The inside diameter of the clutch spring is less than the cycle clutch input hub so that it tightens as the hub rotates. The tip of the

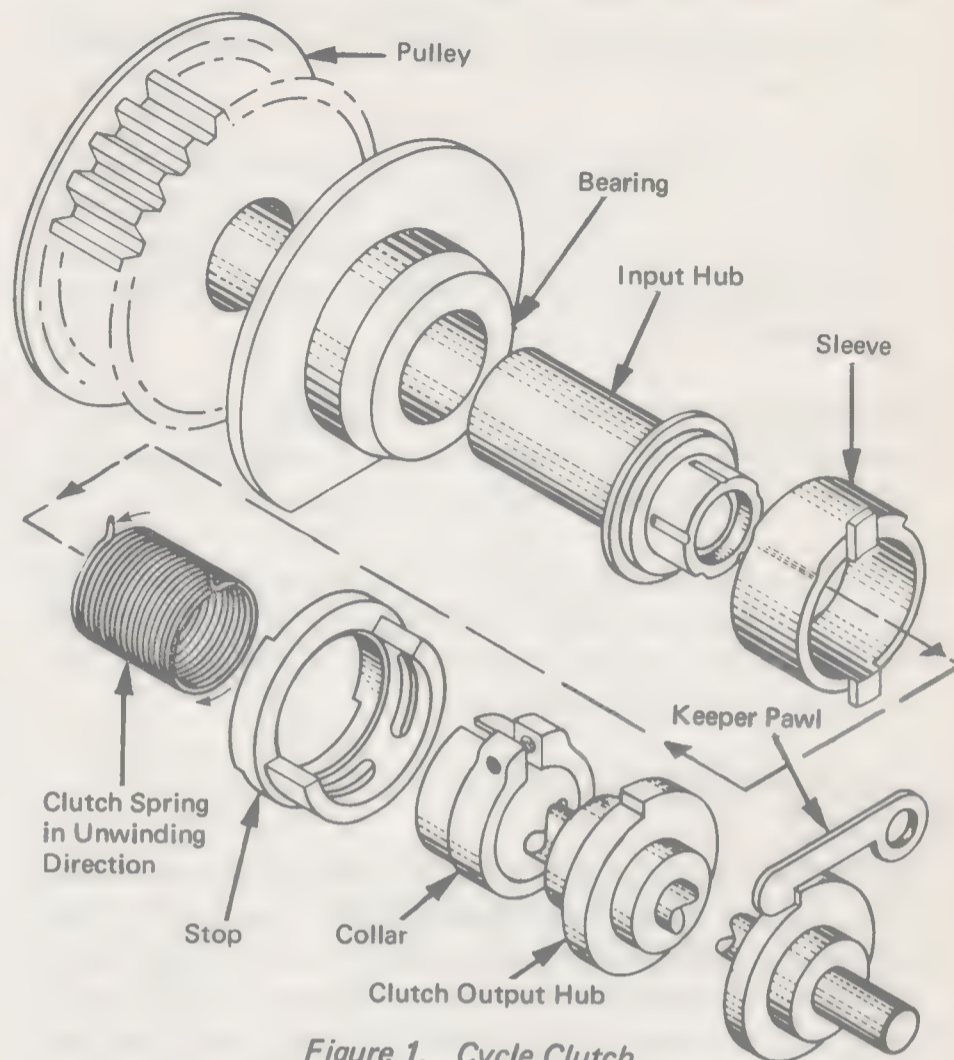


Figure 1. Cycle Clutch

spring is turned out to fit into a notch in the cycle clutch sleeve that encloses the left end of the spring. The clutch sleeve fits loosely around the clutch spring and acts as a control for the left end.

The cycle clutch sleeve that controls the left end of the clutch spring has a step in it. When the clutch drives the cycle shaft, the step of the clutch sleeve contacts the tip of an armature in front of the sleeve (Fig. 2). This is the cycle clutch magnet armature. It stops rotation of the clutch sleeve and thereby stops the left end of the clutch spring. The right end of the spring is rotated farther because of the momentum of the cycle shaft. This additional rotation is in the unwinding direction of the clutch spring, and the spring is enlarged enough to slip.

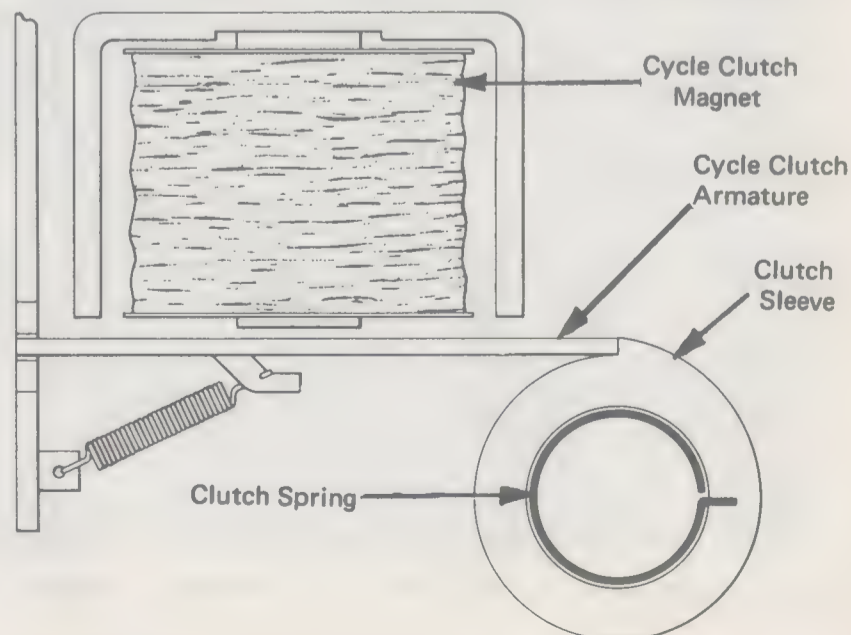


Figure 2. Cycle Clutch Magnet

A certain amount of force must be applied to enlarge the clutch spring. This same force causes the cycle shaft to attempt to creep backward and close up the spring. To prevent any backward creep, the keeper drops into the step in the cycle clutch keeper cam at the other end of the cycle shaft (see Fig. 1). The keeper drops in when the shaft has rotated far enough to disengage the clutch.

The cycle clutch stop is attached to the collar. When the momentum carries the cycle shaft far enough to unlatch the clutch, the stop contacts two lugs on the side of the clutch sleeve and prevents overthrow. Excessive overthrow causes the shaft to stop in an erroneous position.

Energizing the cycle clutch magnet attracts the armature out of the path of the clutch sleeve. The clutch spring quickly decreases in diameter because of its own spring tension.

The rotating cycle clutch pulley hub then tightens the spring and drives the cycle shaft. After the clutch rotates 360 Deg., the sleeve again contacts the armature, if the magnet is de-energized, to disengage the clutch.

### PAPER TAPE SENSING (FIG. 3)

Paper tape is sensed by eight spring loaded sensing arms operating eight corresponding permissive make contacts. A flat steel spring pushes against a pad on the sensing arm to push the tip of the arm through a hole in the paper tape (Fig. 4). The arm pivots around a shaft, moving the tail of the arm down to transfer the permissive make contact. If there is no hole in the paper tape, the paper stops the sensing arm before the contact transfers.

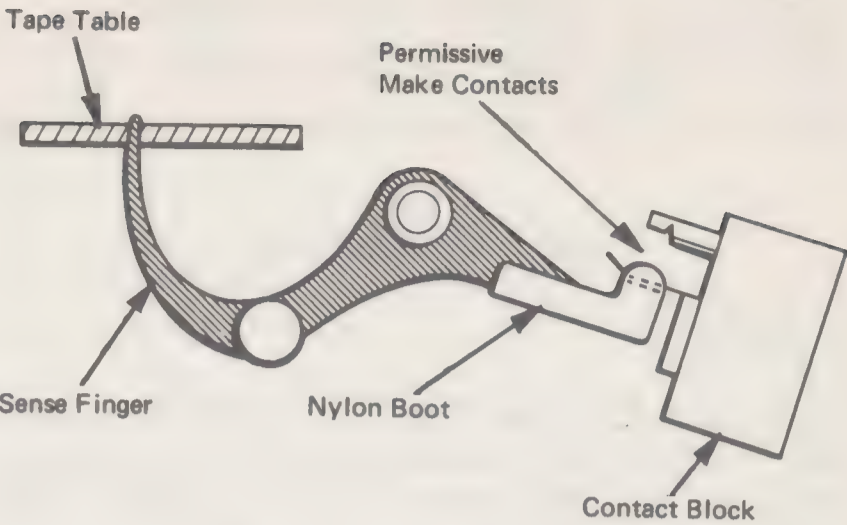


Figure 4. Paper Tape Sensing

After the character is read, the sensing bail pushes against the tail of the sensing arms, and pivots the tips away from the paper tape. The sensing bail cam (see Fig. 3) on the cycle shaft controls the timing of the sensing bail. The cycle clutch is latched up with the sensing bail, and holds the sensing arms away from the paper tape. At the beginning of the cycle, the bail moves down, and allows the sensing arm to pivot into the tape.

### PAPER TAPE FEEDING

The two feed wheels that control the tape motion are driven by a gear attached to the forward feed ratchet (Fig. 3). When the tape is not being moved, a spring loaded roller detent engages the teeth of the thumbwheel to hold it in place. The detent pivots on an eccentric stud which is adjusted to hold the feed wheels with the holes in the paper tape located over the sensing arms.

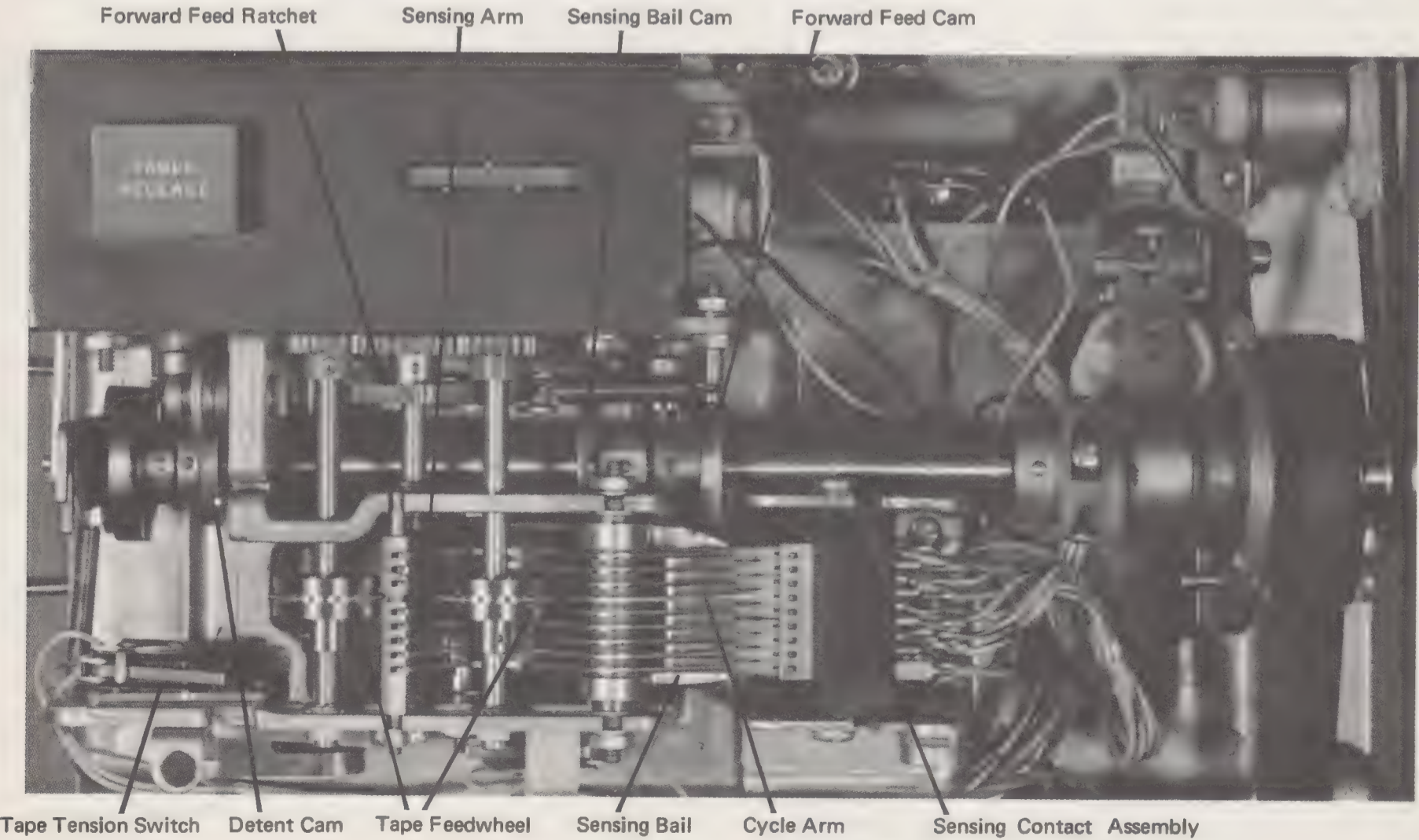


Figure 3. Paper Tape Sensing Unit

As the forward feed cam turns, the cam follower moves into the low dwell and pivots as shown in Figure 5. The pawl on the end of the forward feed cam follower engages a tooth in the forward feed ratchet and moves the ratchet one position (Fig. 6). The feed pawl contacts the stop block to lock the feed ratchet and prevent inertia from moving the feed ratchet too far.

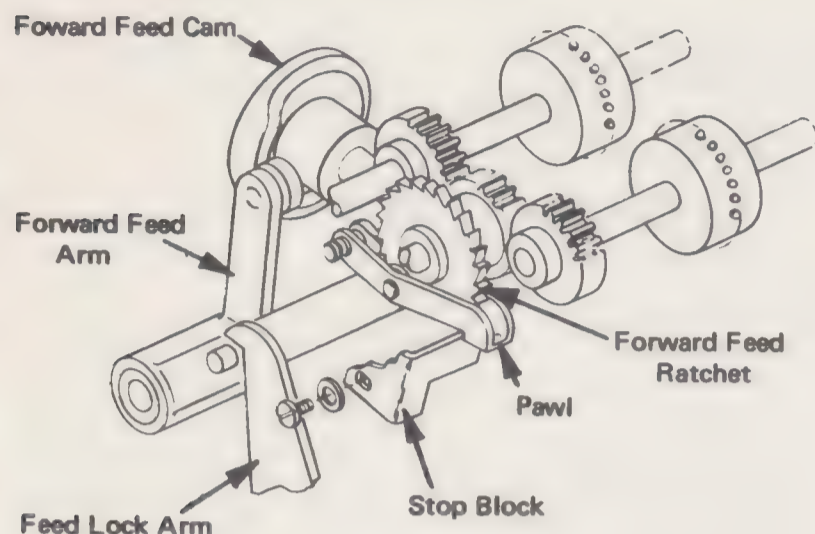


Figure 5. Forward Feed Mechanism

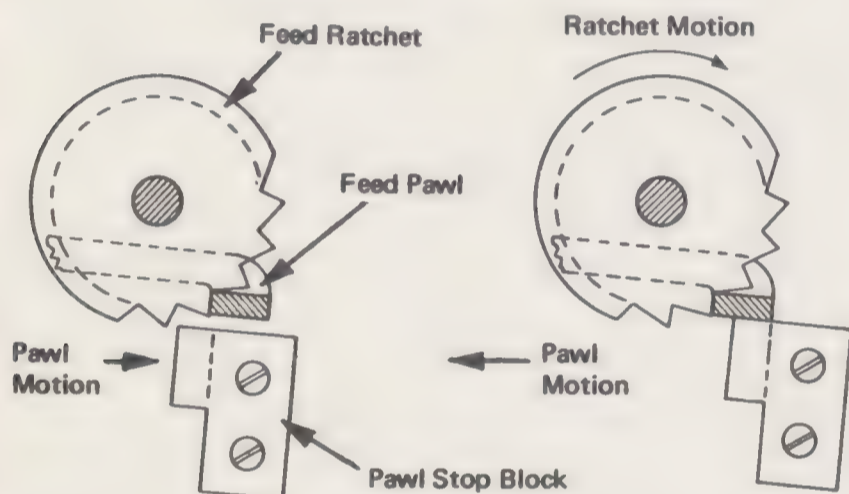


Figure 6. Feed Ratchet

## MISCELLANEOUS

### PAPER TAPE TAKE-UP REEL

The take-up reel is plugged into the drive pulley that is driven from the reader clutch pulley via a belt.

### THUMBWHEEL

This wheel enables the operator to position the paper tape manually.

### TABLE RELEASE

Pressing this key causes the tape table to rise out of the reading position, to permit the insertion or removal of the paper tape.

### TAPE CONTACT AND LEVER

The tape contact is transferred when the paper tape is in position to be read. There are two extensions on the tape lever. When paper tape is read, only the one extension is held down by the tape. The contact opens with about one inch of tape left.

### TAPE TENSION SWITCH (FIG. 3)

This is a normally closed switch, which is opened if the paper tape does not feed freely into the reader.

### CYCLE ARM STROBE CONTACT (FIG. 3)

The cycle arm strobe contact is a permissive make contact operated by a part similar to the sensing arms, but without the tip. This is the cycle arm. It is in the position under the tape feed wheels (Fig. 3). Because there is no tip on the arm, it always pivots enough to transfer its contact. The resulting pulse, called cycle arm strobe, signals the CCU that a character position is being sensed.

### PAPER TAPE READER LOGIC

The program step format for Input from Paper Tape is shown below.

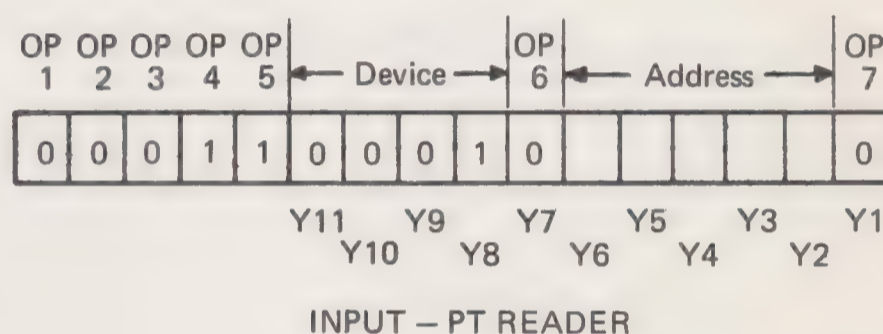


Figure 7. Paper Tape Logic

Input from PT Reader is similar to input from MT Reader. The same "I" Times will be used to perform the step. The cycle clutch logic used during I-5 Time will be different and the feedback signals are different. The codes read from the tape are set in an additional set of latches prior to being transferred to the CCU. These eight latches are called the PT Data Latches.

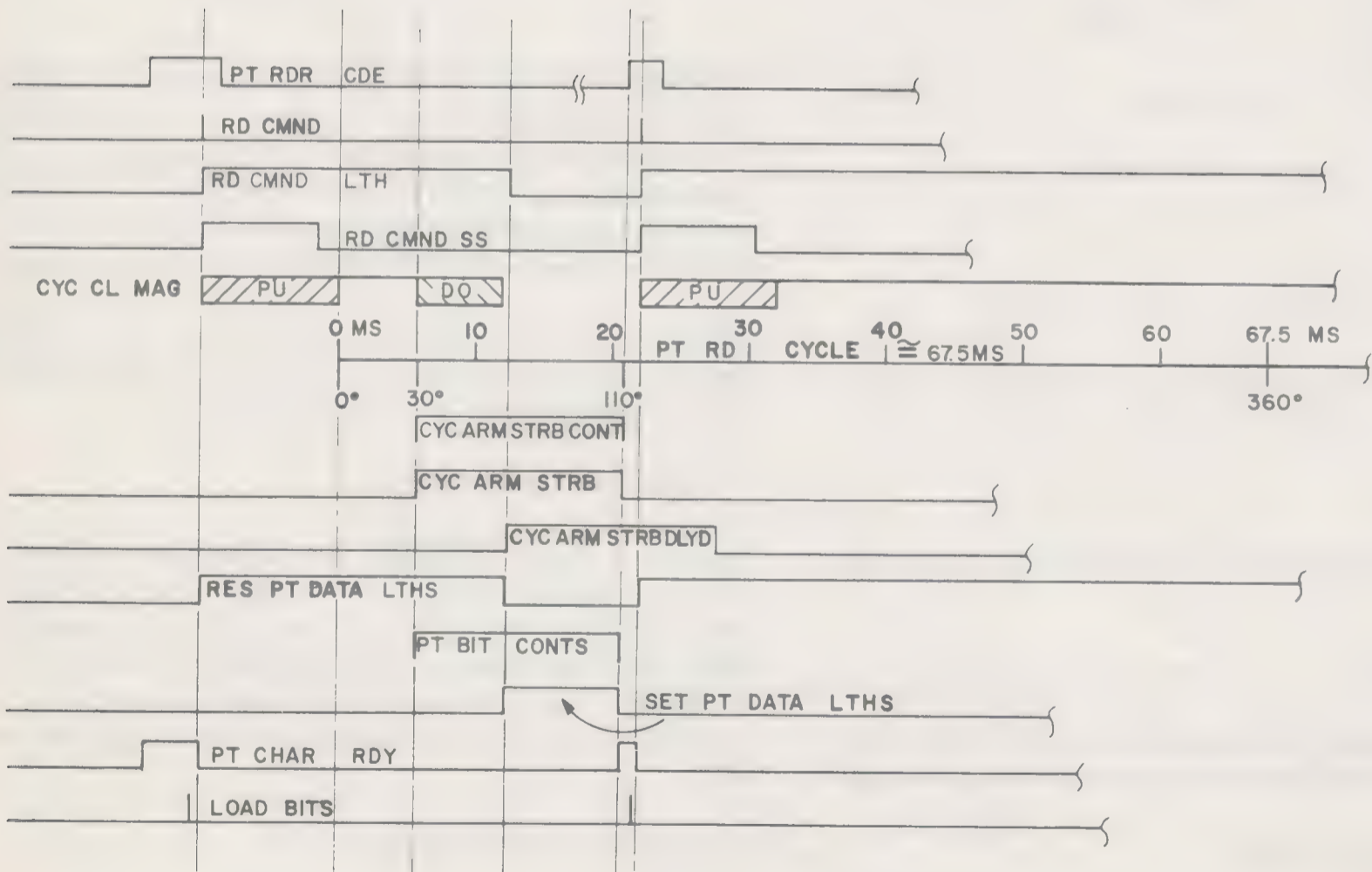
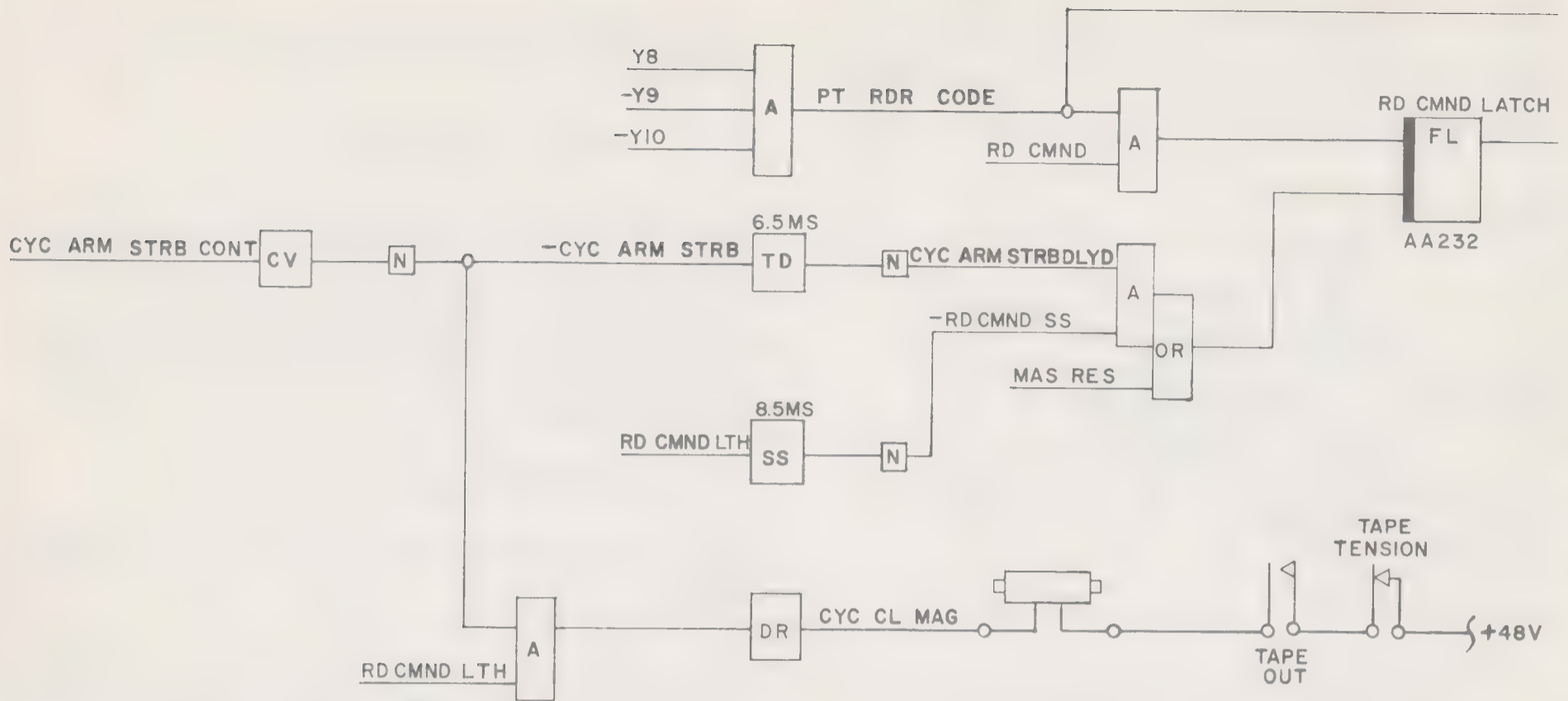
During I-0 and I-1 Times, the program step is located and read as usual. At the end of I-1 Time, the Operational Code Latches will identify the input program step.

### I-2 TIME (P-ONLY CYCLE)

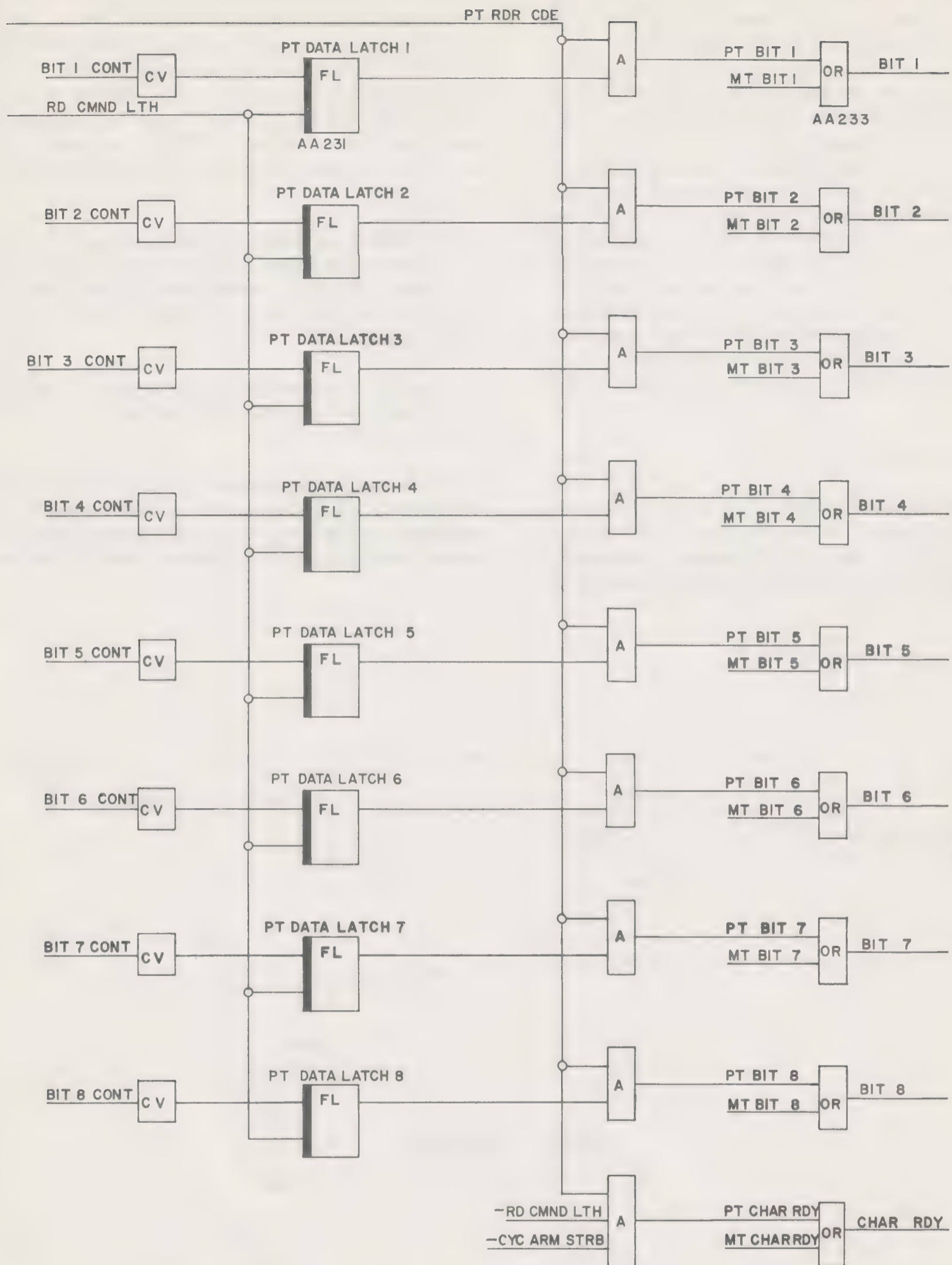
During I-2 Time, the program step will be read from the A-Word and the MAL loaded. Y2-Y6 will be loaded to define the low order address and Y8, Y9, and Y10 will be loaded to define the input device. In our case, the PT Reader will be identified by Y8, -Y9, and -Y10. As you can see, this is also a normal I-2 Time, except for defining a different input device.

### I-5 TIME (P-ONLY CYCLE)

If a character is ready in the PT Data Latches, the Character Ready signal will be up. During I-5 Time, this character will be transferred to the selected low order register. If Character Ready is down, the CCU will be "hung up" in the Input Step by Inhibit until such time as a character is ready.



PT READER TIMING CHART



DATE	E.C. NO.	DATE	E.C. NO.	PAPER TAPE READER LOGIC AND TIMING DIAGRAM	
				PART NO. 1202488	PAGE NO. 0313
				IBM 6320/6354	

0313

The PT Reader cycle clutch will be energized during I-5 Time. Input Strobe comes up at I-5, Central Bit Time of the input step if Not Inhibit and Not Keyboard Code are up. At Bit 13/16 Time, Input Strobe will bring up Read Command. PT Code is ANDED with Read Command to set the Read Command Latch. If the PT Reader is ready, Not Cycle Arm Strobe will be up. Read Command Latch and Not Cycle Arm Strobe will turn on the PT Reader cycle clutch magnet driver and a PT Reader cycle occurs. Two interlock contacts are used to prevent picking the cycle clutch if the paper tape has not been properly inserted or binds so it will not feed. These contacts are in series with the 48 volt supply to the cycle clutch and magnet driver. The normally open Tape contact is held closed if the tape is in position to be read. The normally closed Tape Tension Contact (switch) will be opened if too much tension builds up on the tape. The Tape contact also serves as an end of tape indication — opening as the last inch of tape starts feeding.

### TAPE READER CYCLE

At 30 degrees of the PT Reader cycle, the sensing arms move up under spring tension. If a hole is located above the sensing finger, it will not be stopped by the tape and the associated permissive-make contact will close. This contact brings up an

integrated signal which goes to the set leg of a PT Data Latch. At the same time, the Cycle Arm Strobe contact will make to bring up an integrated signal called Cycle Arm Strobe. Cycle Arm Strobe feeds a time delay circuit to produce Cycle Arm Strobe Delayed 6.5 milliseconds later. Cycle Arm Strobe Delayed will reset the Read Command Latch which removes the reset on the PT Data Latches. The PT Data Latches will now be set by the integrated signals from the permissive-make contacts.

At 110 degrees, the Cycle Arm Strobe contact will open as the sense arms and fingers are restored. The Cycle Arm Strobe signal goes down. Not Cycle Arm Strobe and Not Read Command Latch will turn on PT Character Ready to bring up Character Ready.

With Character Ready up, the character in the PT Data Latches will be transferred to the CCU P-Buffers and written into the selected register at I-5 Time.

At 150 degrees, the cam follower starts down the slope of the low dwell on the feed cam. The tape begins stepping at approximately 200 degrees. Around 280 degrees, the tape has stepped completely as the cam follower reaches the low dwell.

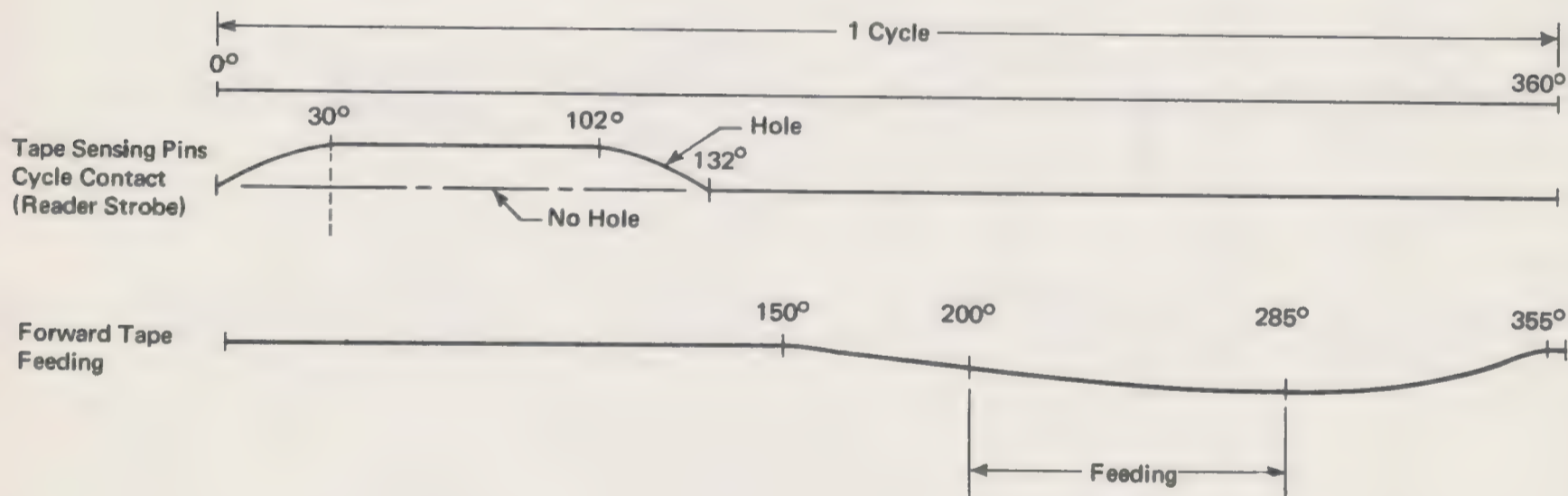


Figure 8. Timing Chart

## RECORD ONLY MT/SR

### INTRODUCTION

The Model V MT/SR is a record only, single station machine. It provides the customer with an economical means of recording tapes for the MT/SC Reader.

The relays used in previous MT/ST's have been replaced by seven SLD cards. These SLD cards are located on a "Half Board" which is mounted to a SLD gate that pivots on the machine frame behind the front panel.

The three console keybuttons function as follows:

Line Return	Backsteps the tape to the last recorded Carrier Return code.
Load	Mechanically unlatches the unload button and initiates the Load operation.
Unload	Mechanically latches down and controls the unload operation.

The Console Lights indicate:

On	Power on.
Ready	Primarily that the machine is ready to record. It is also used during head alignment.
Error	Glow for parity error on the tape. Also used during head alignment.

The Record/Type switch simply places the machine in the desired mode. In the Record mode the information from the I/O will be recorded on the tape. In the Type mode the I/O may be used as a normal "Selectric" typewriter.

In both the Tape Deck and the I/O, several components have been eliminated that are not necessary for the Record only operation.

The text for the MT/SR Model V is written to be read while referring to the ILD's and Function Charts for the operation discussed. These diagrams are fold-out sheets located in the Logic Diagram section of this manual.

### RECORD

The Model V Record operation is basically the same as on the Model II or Model IV MT/ST. The information from the transmit contacts of the I/O is stored in the Buffer latches. The information is then placed on the tape serially by combining the output of the Buffers with the MP's. A parity check is made on the Backstroke to insure an odd number of bits on the tape.

With the Record/Type switch in the Record position and a tape loaded on the machine, a Record operation is possible.

### Logic

Depressing a character keybutton on the I/O causes the I/O cycle clutch to be released and an I/O cycle begins.

When C 1 N/C opens, it drops the electronic signal C 156 N/C, C 1 N/O makes and brings up the C N/O signal.

The RECORD 1 latch is set by Record, —C 156 N/C, —Load 2 or Counter 31-60, —Record 2, —Leader Sense Long, C N/O, —Beginning of Tape, —Load 1 or Counter 16-45 and —Load Search. When Record 1 comes True, —Record 1 goes False and drops BR (Buffer Reset). +48 VDC is supplied through C 1 N/O and the I/O transmit contacts to the CV (Converter). The CV changes this +48 VDC level to a +12 VDC level. This 12 VDC level is used to set the Buffer latch for the corresponding transmit contact.

The console CC magnet is picked with the Record 1 and —CB 8 signals being True. The CC magnet is dropped when CB 8 makes at 38 Deg. of the Console cycle.

MP 1 is generated at 47 Deg. of the forestroke, RECORD 2 latch is set at this time by CB 8, Record 1 and MP 1 being True.

MP2 is generated and at this time we reset Record 1 latch because MP 2 and Record 1 are True.

Magnetic Pickups 3 through 11 are used to record the bits on the tape. The MP to BIT relationship is the same as the Model II or Model IV MT/ST.

By referring to the Function Chart you can see that at MP 3 time if Buffer R1 is set and —Counter 8 is true, then WRITE will come True. When Write comes True, WRITE COIL will also come True provided Record, CB 8, —Error Correct, —Line Return 1 and —Line Return 2 are True. When Write Coil comes True, this causes the current in the WRITE/ERASE head to reverse and thereby record a bit on the tape. MP5 and Buffer R2A or MP6 and Buffer R5 will function the same as MP3 and Buffer R1.

At MP 4 time if Buffer R2 is set, Write will come True. Write Coil will come True with Write, provided its other conditions are satisfied. This will result in a 2 Bit being recorded. MP 8 and Buffer T1 or MP 9 and Buffer T2 function the same as MP 4 and Buffer R2.

At MP 10 time, a Check Bit will be recorded if it is needed to satisfy the odd bit parity requirement. The Check Bit logic is shown on the Function Chart. If Buffer CK is True, —Buffer UC is True and —Reference is True, a CK Bit will be recorded

at MP 10 time. Also if —Buffer CK is True, Buffer UC is True and —Reference is True a CK Bit will be recorded.

On the other hand, if Buffer CK is True and Buffer UC is True, The CK Bit will not be recorded. Also, if —Buffer CK and —Buffer UC are both True, the CK Bit will not be recorded.

At MP 11 time, if Buffer UC is True and —Reference is True, a Shift Bit (8 Bit) will be recorded.

At 144 Deg. of the console cycle the record portion of the cycle is complete. CB 8 opens and —CB 8 comes True. C N/C and —CB 8 reset Record 2. —Record 1 and —Record 2 being True bring up BR. BR coming True resets the Buffers.

MP 1 is generated at 238 Deg. of the Backstroke. MP 1 and —CB 8 being true bring up BACKSTROKE. Backstroke —CE Aid, —Line Return 2 and —Error Correct pick the Forestep Magnet.

On the Backstroke as the head sweeps toward home, the bits are sensed by the READ AMP and combined with Backstroke and —Reference to generate a signal called CRT AC (Counter AC). Each time CTR AC comes True, Counter 1 will change state. At MP 1 time on the backstroke we reset the counter to zero (all counters off). If we begin with Counter 1 off and read an odd number of bits, then Counter 1 will be on at MP 11 time. Home Switch will make at 340 Deg. and bring up the signal HOME SW. Home Sw and —Reference bring up COUNTER RESET and this resets the counter to zero. Because —Home Sw went false, we drop Backstroke. Backstroke going false drops the Forestep magnet.

If an even number of bits were read during the backstroke, then Counter 1 would be off at MP 11 time. With MP 11, —Counter 1, —Reference, —Error Correct, —Load 2 or Counter 31-60, —Line Return 1 and Backstroke all True, the ERROR latch would set. Error being True would turn on the Error Light. With Error and Record True, the Keyboard Lock Solenoid would pick and mechanically lock the I/O keyboard. This would indicate to the operator that an error had been made in recording.

## LOAD OPERATION

The Load Operation will advance the tape to the first recordable tract. The tape will be advanced at a high speed until the Beginning of Tape slot is sensed and then stepped each cycle until a feed code is recorded.

### Logic

Depressing the Load keybutton causes the Load Sw N/O to make. LOAD is an integrated signal that comes True when Load Sw N/O makes. 48V is supplied to the Load Search and Detent Solenoids through the Record Sw N/O. The ground for the Load Search solenoid is through the Load Sw N/O, Reel Interlock Sw N/O and Leader Sense Long Sw N/C. The detent solenoid is picked through the Beginning of Tape Sw N/O, End of Tape Sw N/O, Unload Sw N/C, Load Search Sw N/O and

the Home Sw N/O, LOAD 1 or COUNTER 16-45 is set by Load Search, Load and Leader Sense Long.

With the Detent out of the ratchet and the Load Search shaft shifted, the tape will load at a high speed until the Beginning of Tape Sw N/O opens and drops the Detent solenoid and the Load Search solenoid. When the Beginning of Tape Sw N/C makes, it brings up a signal called BEGINNING OF TAPE. Load Search Sw N/O opening causes Load Search to drop. Beginning of Tape, —Load Search and Load 1 or Counter 16-45 set LOAD 2 or COUNTER 31-60.

Load 1 or Counter 16-45, Load 2 or Counter 31-60 and —CB 8 provide one circuit to pick the Console CC. These conditions will be used to pick the CC each cycle until the Beginning of Tape Sw N/C opens.

CB 8 makes at 38 Deg. and an electronic signal called CB 8 comes True. Because —CB 8 goes false, the CC magnet is dropped.

The machine will attempt to record a Feed code on the tape at MP 3, MP 5, and MP 9 times. MP 3, MP 5, and MP 9 are ANDED With Load 2 or Counter 31-60 and —Reference to bring up WRITE. Write is then ANDED with Record, CB 8, —Error Correct, —Line Return 1 and —Line Return 2 to bring up WRITE COIL. When Write Coil comes True, the current in the WRITE/ERASE winding of the Read/Write head is reversed for the duration of MP 3, MP 5 or MP 9.

CB 8 opens at 144 Deg. At this time, if the Beginning of Tape Sw N/C is still made (the roller in the slot), the CC will be re-picked.

MP 1 on the backstroke is generated by 238 Deg. With —CB 8 and MP 1 True, BACKSTROKE will come True. The Forestep magnet will be picked with Backstroke, —CE AID, —Error Correct and —Line Return 2.

MP 1 is also ANDED with Record, —CB 8 and —Reference to bring up COUNTER RESET. Counter Reset will reset the counter to zero (all counters off).

As the head sweeps on the backstroke the bits are sensed by the READ AMP and ANDED with —Reference and Backstroke to bring up CTR AC (Counter AC). Each time CTR AC comes up, Counter 1 will change state.

MP 11 on the backstroke is generated at 317 Deg. At this time, a Parity Check is made by checking the state of Counter 1. If Counter 1 is off, an even number of bits were read. If Counter 1 is on, an odd number of bits were read and Parity is correct.

Consider the tape stepped until the Beginning of Tape Sw N/C opens (roller out of the slot) and the head still over blank tape. Counter 1 will be reset at MP 1 time on the backstroke and remain off since no bits are read to change its state.

Home Switch will make at 340 Deg. and bring up the signal Home Sw. Home Sw is ANDED with —Reference, —Beginning of Tape and Load 2 or Counter 31-60 to reset Load 1 or Coun-

ter 16-45. The CC magnet is now picked with Home Sw and Load 2 or Counter 31-60 and the machine will continue to attempt to record a Feed code.

When the tape is stepped far enough for the head to pass over the oxide portion of the tape, a Feed code will be recorded. With a Feed code recorded, let's begin at MP 1 time on the backstroke and complete the cycle.

MP 1 and —CB 8 bring up Backstroke. Backstroke, —CE AID, —Error Correct and —Line Return 2 pick the Forestep magnet. MP 1, Record, —CB 8 and —Reference bring up Counter Reset. Counter Reset resets the counter to zero.

As the head sweeps toward home on the backstroke, the first bit sensed by the Read Amp will be the 5 bit. Read Amp will come True when the 5 bit is sensed and with —Reference and Backstroke already True, CTR AC will come True. Counter 1 will turn on when the 5 bit is read, off when the 3 bit is read and on again when the 1 bit is read.

With Counter 1 on (odd parity) at MP 11 time of the backstroke, we have —Reference, —Load 1 or Counter 16-45, Counter 1, Backstroke and MP 11 used to reset Load 2 or Counter 31-60. The CC will not repick since Load 2 or Counter 31-60 is reset.

At 340 Deg., Home Sw comes True. Home Sw and —Reference bring up Counter Reset which resets the counter to zero. Home Sw resets Backstroke which drops the Forestep magnet and the Load Operation is complete.

## ERROR CORRECT

Should an even number of bits be read during the backstroke of a Record cycle, the ERROR latch would be set. The Error latch coming True will cause the ERROR LIGHT to glow and the KEYBOARD LOCK SOLENOID to pick.

The Error latch can be reset with an I/O backspace operation or a Line Return operation. In the case of an I/O Backspace operation, the ERROR CORRECT latch will be set which in turn will reset the Error latch and Backstep the tape. If Line Return is used, the Line Return 1 latch will set and this will cause the Error latch to reset. The Line Return logic is discussed in detail in the Line Return operation. The following logic pertains only to the I/O Backspace/Error Correct operation.

### Logic

Depressing the Backspace key on the I/O will cause a normal Backspace operation on the I/O. Also, C-5 N/O will transfer and bring up the C N/O signal and the —C 156 N/C signal.

RECORD 1 latch will set when C N/O, Record, —Beginning of Tape, —Load 1 or Counter 16-45, —Record 2, —Load Search, —Leader Sense Long, —Load 2 or Counter 31-60 and —C 156 N/C are True.

BR (Buffer Reset) will drop when —Record 1 goes False. At

this time the Buffers R2A, R5 and T2 will set through the Backspace Transmit contacts and C 5 N/O.

The Console CC magnet will be picked by Record 1 and CB 8 being True.

The ERROR CORRECT latch will be set by Record 1, —Buffer R1, —Buffer R2, Buffer R2A, Buffer R5 and CB 8 being True. Error Correct being True will reset the Error latch. Error latch going false will drop the Error Light and the Keyboard Lock Solenoid. The Console CC will also drop when —CB 8 goes false.

MP 1 is generated at 47 Deg. of the forestroke. At this time, Record 2 will be set by MP 1, Record 1 and CB 8 being True.

As the Emitter sweeps MP 3 through MP 11 Write Coil is inhibited by the Error Correct latch being True. This prevents any current flow in the Write/Erase Winding; therefore, the tape is not erased nor is the Backspace code recorded.

CB 8 opens at 144 Deg. and —CB 8 comes True. Record 2 resets with C N/C and —CB 8 being True.

MP 1 is generated at 238 Deg. of the backstroke. The BACKSTROKE latch sets with —CB 8 and MP 1. Error Correct and Backstroke being True cause the Backstep magnet to pick. The Forestep magnet is inhibited by —Error Correct being false.

The Home Switch makes at 340 Deg. and brings up the signal HOME SW. Home Sw being True resets the Backstroke latch and the Error Correct latch, either of which will drop the Backstep magnet.

The Error latch has been reset. The Error Light is off and the I/O keyboard is unlocked. The tape has been Backstepped so that when the information is recorded again, the error will be corrected.

## LINE RETURN

The Line Return operation allows the operator to return the tape to the last previously recorded Carrier Return code.

### Logic

Referring to the Function Chart you will notice that LINE RETURN 1, set when Line Return N/O comes true, initiates the first cycle. LINE RETURN 2 is set during the backstroke and Line Return 1 cannot be reset until Line Return 2 is True. Therefore, a carrier return code read during the first cycle will not stop the Line Return operation.

Another condition required to reset Line Return 1 is —Decode 1 being True at the end of MP 8 time. —Decode 1 will be True at this time only if a 3 bit alone was sensed by the Read Amp.

With this information in mind, let's proceed with a detailed discussion of the ILD's and Function Chart.

Depressing the Line Return keybutton causes the Line Return

switch N/O to make and bring up the LINE RETURN N/O signal.

Line Return 1 will be set by Record, —Reference, —Load 1 or Counter 16-45, —Load Search, —Counter 8, —Leader Sense Long, —Load 2 or Counter 31-60, —Line Return 2 and Line Return N/O.

Line Return 1 and Record pick the High Bias magnet. Line Return 1 and —CB 8 pick the CC magnet. The CC magnet will repick each cycle at 144 Deg. until Line Return 1 is reset.

MP 1 is generated at 238 Deg. of the backstroke. At this time, the Line Return 2 latch will be set by MP 1, —CB 8 and Line Return 1.

BACKSTROKE comes True with MP 1 and —CB 8. The Backstep magnet is picked by —CE AID, Backstroke and Line Return 1. The Forestep magnet is inhibited by —Line Return 2 being False.

Decode 1 is a bi-stable trigger that has a DC reset leg tied to the Home Sw. Anytime Home Sw is True, Decode 1 will be reset, but Home Sw is False between 20 Deg. and 340 Deg. With Home Sw false, an AC input to Decode 1 will cause it to change state if the other AND conditions are satisfied.

Decode 2 has a DC reset leg that is tied to —CB 8. —CB 8 will be False between 38 Deg. and 144 Deg. During this time, Decode 2 will respond to its inputs provided all AND conditions are satisfied.

A 1 and/or 2 bit sensed will set Decode 1. The conditions are CB 8, Read Amp and —Decode 2 being True. Decode 1 will remain True until Home Sw comes True at 340 Deg. Since —Decode 1 must be True at the end of MP 8 time to reset Line Return 1, the Line Return operation continues.

If a 1 or 2 bit is not sensed, at the end of MP 3 time Decode 1 and Decode 2 will be set. The positive shift of —MP 3 is AND-ED with —CE AID and —Decode 1 to set Decode 2. Decode 1 is set by CB 8, —CE AID and the positive shift of —MP 3.

If a 3 bit is sensed, Decode 1 will be reset by CB 8, Read Amp and Decode 2.

At the end of MP 4 time, Decode 2 will be reset by —CE AID and the positive shift of —MP 4.

If a 4, 5, or 6 bit is sensed, Decode 1 will be set again by CB 8, Read Amp and —Decode 2. Decode 1 will be True at the end of MP 8 time and will not satisfy the conditions to reset Line Return 1.

If a 4, 5, or 6 bit is not sensed, Decode 1 will remain reset and —Decode 1 will be True at the END OF MP 8 time. This END OF MP 8 pulse is a 10 microsecond positive pulse. It is generated by delaying an MP 8 pulse 10 microseconds and ANDING it with —MP 8.

Line Return 1 will reset with —Decode 1, End of MP 8, Line

Return 2 and CB 8 being True. The High Bias, CC and Backstep magnets are dropped when Line Return 1 goes False.

Line Return 2 is reset at 340 Deg. by Line Return N/C, —Line Return 1 and Home Sw.

## COUNTER

A Binary type counter that has 16 stable conditions is used. Each counter is a bi-stable trigger that changes state with a positive shift input. Its primary function is control of the Encode Reference cycles. Part of the counter is also used in Error Check and Head Alignment operations.

The Counter Reset signal will turn all counters off. We say "Reset to Zero" or "Zero in the Counter" when the counter has been reset.

The CTR AC (Counter AC) signal is applied to Counter 1. With all counters off (Zero in the Counter) the output of the lower portion of Counter 1 is positive (True). This is tied back to the input of the upper portion of Counter 1. When CTR AC comes True, both conditions of the AND circuit for the upper portion of Counter 1 will be satisfied and Counter 1 will turn on. A negative shift is felt at Counter 2 input through the coupling capacitor. A positive shift is required at the input to change the state of Counter 2 so the negative shift will not change the state of Counter 2.

Now with Counter 1 on we have "1" in the counter. The Counter 2 lower output is positive and is fed back to the AND circuit for the upper portion of Counter 2. When CTR AC goes positive again, the AND circuit for the lower portion of Counter 1 will be satisfied and Counter 1 will change state. When Counter 1 turns off, the output of the lower portion of Counter 1 goes positive. This positive shift is felt through the coupling capacitor to Counter 2. The positive shift from the lower portion of Counter 1 ANDs with the positive output of the lower portion of Counter 2 to satisfy the AND circuit for the upper portion of Counter 2. The upper portion of Counter 2 will turn on and now we have Counter 1 off and Counter 2 on or "2" in the counter.

When Counter 1 turns on again, a negative shift is felt at Counter 2. This does not change the state of Counter 2, so we now have Counter 1 and Counter 2 on or "3" in the counter.

When Counter 1 turns off with the next CTR AC pulse, a positive shift will be felt to Counter 2 which will turn it off. Counter 2 turning off will feed a positive pulse to Counter 4 which will cause the upper portion of Counter 4 to turn on. We now have Counter 1 off, Counter 2 off, and Counter 4 on or "4" in the counter.

You can see that in the 15th cycle the counter will step to 15. All counters will be on at the end of the 15th cycle.

When the CTR AC signal is generated on the 16th cycle, Counter 1 will turn off. A positive shift from Counter 1 turns Counter 2 off. A positive shift from Counter 2 turns Counter 4 off. A positive shift from Counter 4 turns Counter 8 off. At the end

of the 16th cycle, all counters are off and we have "0" in the counter.

By using the latches Load 1 or Counter 16-45 and/or Load 2 or Counter 31-60 with the counter outputs, it is possible to control the bits recorded during the Reference sequence.

## PREFIX CODE

The operator may record a PREFIX CODE by simply depressing the PX key located just to the left of the tab set and clear keybutton. The bit configuration for a Prefix Code is the same as a Stop Code (1, 3, 4 bits). The console will cycle and record the Prefix Code. Also, the Red Ribbon Mag will be picked so that the next character printed will be in red.

A REFERENCE CODE is recorded by depressing the "X" keybutton after a Prefix Code has been recorded. The "X" will print in red. The information on the tape will be Prefix Code / "X" / Reference Code (15AS, 15 Search, 30 CK, 1 CR). The Reference Code will not be followed by a comma since the MT/SC read operation is different from the search operation.

## Logic

Depressing the Prefix Key on the I/O causes Prefix 1 Sw N/O to make. This causes the C N/O signal to come true and the C N/C signal to go false, but does not affect the C 156 N/C signal which remains true.

PREFIX RECORD 1 will be set with C N/O, C 156 N/C, —Prefix Record 2, —Reference, —Counter 8, Prefix Record 1 will pick the RED RIBBON MAGNET in the I/O.

RECORD 1 will be set with Record, C N/O, —Record 2, —Load Search, —Load 1 or Counter 16-45, —Load 2 or Counter 31-60, —Leader Sense Long, —Beginning of Tape and —Prefix Record 2. BR (Buffer Reset) will drop because —Record 1 goes false. Buffers R1, R2A and R5 will now set with Prefix 1 Sw N/O. Record 1 and —CB 8 pick the Console CC Magnet.

At 38 Deg. CB 8 makes and because —CB 8 goes false, the CC Magnet is dropped.

MP 1 is generated at 47 Deg. RECORD 2 will set at this time with Record 1, MP 1 and CB 8 being true.

RECORD 1 will be reset at MP 2 time of the forestroke by MP 2 and Record 2 being true.

MP 3 and Buffer R1 combine with —Counter 8 to bring WRITE true. WRITE COIL will come true with —Error Correct, —Line Return 1, —Line Return 2, Write, Record and CB 8. When Write Coil comes true, the current in the Write/Erase Coil will be reversed and a 1 bit recorded. Buffer R2A and MP 5 will record a 3 bit in the same manner. Buffer R5 and MP 6 will record a 4 bit. The emitter will continue its sweep through MP 11.

At 144 Deg. CB 8 will open. Record 2 will be reset by —CB 8 and C N/C. BR will come true with —Record 1 and —Record 2

being true. The Buffers will be reset when BR comes true.

PREFIX RECORD 2 will set with Prefix Record 1, —Record 1, —Record 2 and C N/C being true.

MP 1 on the backstroke is generated at 238 Deg. BACKSTROKE will set with —CB 8 and MP 1 being true. Backstroke, —CE Aid, —Line Return 2 and —Error Correct will pick the FORESTEP MAGNET.

MP 1, Record, —CB 8, and —Reference being true will cause Counter Reset to come true and the Counter will RESET TO ZERO.

As the head sweeps toward home, the output of the READ AMP will be combined with Backstroke and —Reference to cause CTR AC to come true. Each time CTR AC comes true Counter 1 changes state. Counter 1 is turned off at MP 1 time (238 Deg.), so if an odd number of bits were read, Counter 1 will be on at MP 11 time (317 Deg.).

If an even number of bits were read on the Backstroke, Counter 1 would be off at MP 11 time. The Error Latch would be set with MP 11, —Counter 1, —Reference, —Error Correct, —Load 2 or Counter 31-60, —Line Return 1 and backstroke being true. The Error Light will glow and the keyboard lock magnet will be picked by Record being true and —Error being false.

If Counter 1 is on at MP 11 time, then an odd number of bits were read and parity is correct.

Home Sw makes at 340 Deg. and the Home Sw signal comes True. Counter Reset will come True with —Reference and Home Sw being true and this resets the counter. Home Sw being true resets Backstroke which drops the Forestep Magnet.

This completes the Prefix Code cycle. At this time, Prefix Record 1 and Prefix Record 2 are still up and latched. Also, the Red Ribbon Mag is picked. Let's now record a character other than an "X".

## CHAR. FOLLOWING PREFIX CODE (EXCLUDING "X")

Depress the character keybutton on the I/O. C 1 N/C will open causing the C 156 N/C signal to drop. C 1 N/O will make bringing up the C N/O signal.

Prefix Record 1 will be reset by C N/O and —C 156 N/C being True.

Record, C N/O, —Record 2, —Load Search, —C 156 N/C, —Load 1 or Counter 16-45, —Load 2 or Counter 31-60, —Leader Sense Long and —Beginning of Tape being True will set Record 1. When Record 1 comes True, Record 2 goes False and drops BR. The Buffers will be set through C 1 N/O and the transmit contacts.

Record 1 and —CB 8 being True pick the console CC magnet. CB 8 makes at 38 Deg. and —CB 8 goes False and drops the CC magnet.

MP 1 is generated at 47 Deg. of the forestroke. Record 2 will be set by CB 8, MP 1 and Record 1 being True. Also, Prefix Record 2 will reset with MP 1, CB 8, —Prefix Record 1 and Buffers R1 or R2 or R2A or T2 or —T1 or —R5 (anything except "X"). The Red Ribbon Magnet will be dropped when Prefix Record 2 resets.

Record 1 will be reset by MP 2 and Record 2 being True.

The rest of the cycle is identical to a normal Record and Error Check cycle.

#### RECORD "X" FOLLOWING PREFIX CODE

A Prefix Code was recorded in the previous cycle. Prefix Record 1 and Prefix Record 2 are up and latched. The Red Ribbon Magnet is also picked.

Depressing the "X" keybutton will:

1. Print a Red "X" on hard copy.
2. Record an "X" on the tape.
3. Set the Reference Latch.

Depress "X" keybutton. C1 N/O will make and bring up the C N/O signal. Also, —C 156 N/C will come True. Prefix Record 1 will be reset by C N/O and —C 156 N/C. Record 1 will set with Record, C N/O, —Record 2, —Load Search, —Load 1 or Counter 16-45, —Load 2 or Counter 31-60, —Leader Sense Long, —Beginning of Tape and —C 156 N/C being True.

BR will go False when Record 1 becomes True because —Record 1 goes False. Buffers R5, T1 and CK will set through C1 N/O and the transmit contacts.

Record 1 and —CB 8 pick the console CC Magnet.

CB 8 makes at 38 Deg. and because —CB 8 goes False, the CC magnet is dropped.

Record 2 is set MP 1 time (47 Deg.) by MP 1, Record 1 and CB 8.

Record 1 resets at MP 2 time because MP 2 and Record 2 are both True.

Buffer R5, MP 6 and —Counter 8 cause Write to come True. Write Coil will come True with Write, Record, CB 8, —Error Correct, —Line Return 1 and —Line Return 2 being True. When Write Coil comes True, the current in the Write/Erase winding is reversed and in this case a 4 bit is recorded.

Buffer T1 and MP 8 being True will cause a 6 bit to be recorded. Buffer CK, —Buffer UC, —Reference and MP 10 will cause a 7 bit to be recorded.

CB 8 opens at 144 Deg. Record 2 will be reset by C N/C and —CB 8 being True. —Record 1 and —Record 2 being True causes BR to come True and this resets the Buffers.

MP 1 is generated at 238 Deg. of the Backstroke. MP 1 and

—CB 8 set Backstroke. Backstroke, —CE Aid, —Line Return 2 and —Error Correct pick the Forestep Magnet.

MP 1, —CB 8, Record and —Reference cause Counter Reset to come True and this resets the counter to zero.

As the head sweeps toward home on the Backstroke, the Read Amp senses the bits. Since —Reference and Backstroke are already True, each time Read Amp comes True, CTR AC will come True. Counter 1 will change state each time CTR AC comes True.

Counter 1 is reset at MP 1 time (238 Deg.) and with an odd number of bits read on the Backstroke Counter 1 will be on at MP 11 time (317 Deg.).

If for any reason Counter 1 is off at MP 11 time, —Counter 1, MP 11, Backstroke, —Reference, —Error Correct, —Line Return 1 and —Load 2 or Counter 31-60 will set the Error Latch. The Error Light will glow and Record ANDED with Error will pick the Keyboard Lock Magnet.

If an odd number of bits are sensed, then the odd parity is correct and Counter 1 will be on at MP 11 time.

Home Sw makes at 340 Deg. and brings up the Home Sw signal. Home Sw being True resets Backstroke which drops the Forestep Magnet.

The Reference latch will be set with —Prefix Record 1, Prefix Record 2, C N/C, —Record 1 and Home Sw.

Reference and Prefix Record 2 bring Counter Reset True and this resets the counter to zero.

Reference and —CB 8 pick the CC magnet. The CC magnet will repick each cycle when CB 8 opens at 144 Deg. until Reference is reset.

CB 8 makes at 38 Deg. and because —CB 8 goes False, the CC magnet is dropped.

MP 1 is generated at 47 Deg. MP 1, Prefix Record 1, CB 8 and Buffers R1 or R2 or R2A or T2 or —R5 or —T1 reset Prefix Record 2 which drops the Red Ribbon Magnet.

Write will come True at MP 3, MP 5 and MP 9 times because —Load 1 or Counter 16-45, —Load 2 or Counter 31-60 and Reference are True. Write Coil will come True with Write CB 8, Record, —Line Return 1, —Line Return 2 and —Error Correct being True. When Write Coil comes True, the current in the Write/Erase winding will be reversed for the duration of MP 3, MP 5 and MP 9 and a 1, 3 and 6 bit will be recorded respectively.

At 317 Deg. of the Backstroke, MP 11 is generated, MP 11, —CB 8 and Reference being True bring up CTR AC. The Counter will advance 1 for each CTR AC pulse. The Counter was reset at the end of the "X" cycle so now it will advance to 1. You can see from the function chart that we will continue to record Auto Search codes until the Counter is equal to 15.

At MP 1 time (47 Deg.) of the 16th cycle, Load 1 or Counter 16-45 will be set by MP 1, Reference, Counter 1, Counter 2, Counter 4, Counter 8 and —Load 2 or Counter 31-60.

At MP 7 time of the 16th cycle with Reference, Load 1 or Counter 16-45 and —Load 2 or Counter 31-60 being True, Write will come True. Write Coil will come True with Write, Record, CB 8, —Line Return 1, —Line Return 2 and —Error Correct being True. When Write Coil comes True, the current in the Write/Erase winding will reverse and a search bit will be recorded at MP 7 time.

Again we step the counter with CTR AC which comes true with MP 11, Reference and —CB 8. The Counter will step to Zero on the 16th cycle and begin counting to 15 again. You can see from the function chart that we will continue to record search bits until the counter equals 14. This will be the 30th cycle.

At MP 1 time (47 Deg.) of the 31st cycle, MP 1, Reference, —Counter 1, Counter 2, Counter 4, Counter 8 and Load 1 or Counter 16-45 will set Load 2 or Counter 31-60.

Write will come True at MP 10 time because MP 10, Reference and Load 2 or Counter 31-60 are True. Write Coil will come True with Write, —Line Return 1, —Line Return 2, —Error Correct, Record and CB 8. When Write Coil comes True, the current is reversed in the Write/Erase winding and a 7 bit is recorded on the tape.

MP 11 is generated at 317 Deg. of the Backstroke. MP 11, Reference and —CB 8 are ANDED to generate CTR AC. At MP 11 time of the 31st cycle, the counter steps to 15. The Reference cycles will continue recording 7 bits through the 60th cycle.

Load 1 or Counter 16-45 is reset at MP 1 time of the 46th cycle. This is the first time that the counter is equal to 13 since Load 2 or Counter 31-60 was set. Load 1 or Counter 16-45 is reset by MP 1, Counter 1, —Counter 2, Counter 4, Counter 8, Reference and Load 2 or Counter 31-60. This does not change the recording of the 7 bits in any way.

At MP 1 time (47 Deg.) of the 61st cycle, the counter will equal 12. Reference will be reset by MP 1, —Counter 1, —Counter 2, Counter 4, Counter 8, —Load 1 or Counter 16-45 and Load 2 or Counter 31-60. When Reference goes False, the conditions to pick the CC magnet are no longer satisfied and this will be the last cycle (61st).

Load 2 or Counter 31-60 will be reset by MP 2, Counter 8 and —Reference being True.

MP 5, Counter 8 and —Reference are ANDED to bring Write True. Write Coil will come True with Write, Record, CB 8, —Line Return 1, —Line Return 2 and —Error Correct being True. When Write Coil comes True, the current in the Write/Erase winding will be reversed and a 3 bit will be recorded on the tape.

CB 8 opens at 144 Deg. and —CB 8 comes True.

MP 1 at 238 Deg. is ANDED with —CB 8 to bring up Backstroke. Backstroke, —CE Aid, —Line Return 2 and —Error correct pick the Forestep Magnet.

MP 1, Record, —CB 8 and —Reference cause counter reset to come True and this resets the counter to zero.

The 61st cycle of the Reference Code is completed as a normal Error Check cycle.

## ALIGNMENT OPERATION

To align the Read/Write head on the MT/SR Model V to an MT/ST Master Tape, proceed as follows:

### Along The Tape

1. Position the master tape so that the head will read across a sprocket hole in the "A" section.
2. Place the record/type switch in the type position.
3. Place the CE AID Switch in the up or forward position.
4. The console will now "free run" and both the error and ready lights should glow. (Error = 1 Bit ---- Ready = 8 Bit).
5. If both lights do not glow, adjust the tape sprocket eccentric until they do.

### Across the Tape

NOTE: Before attempting the across the tape adjustment, the along the tape adjustment must be correct.

1. Position the master tape so that the head will read across a sprocket hole in the "B" section of the tape.
2. Both the Error and Ready lights should glow if alignment is correct.
3. If only the Error light glows, the 4 bit was read early and the head should be adjusted toward the sprocket hole.
4. If only the Ready light glows, the 5 bit was read late and the head should be adjusted away from the sprocket hole.

## Logic

### Along the Tape

With the Record/Type switch in its Type (N/C) position and the CE AID switch in its up or forward position, the electronic signal CE AID will come True.

When CE AID comes True, it is ANDED with —CB 8 to pick the CC magnet. Since —CE AID is False, stepping is inhibited.

If a 1 bit is sensed, Decode 1 will be set by read amp, CB 8 and —Decode 2. When CB 8 opens at 144 Deg. the error light will glow because —CB 8, —Line Return 1 and CE AID are all True.

If a 1 bit is not sensed, Decode 1 and Decode 2 are both set by the positive shift of —MP 5. At MP 6 time, Line Return 1 will be set by CE AID, MP 6 and Decode 2 being True. Line Return 1 being True at 144 Deg. will inhibit the Error Light.

At the end of MP 6 time when —MP 6 goes positive, —Decode 2 will be reset and counter 1 will be turned on.

If an 8 bit is sensed, Counter Reset will come True because CE AID, CB 8 and Read Amp are true. Counter Reset will turn Counter 1 off. At 144 Deg. the Ready light will come on because CE AID, —CB 8 and —Counter 1 are True.

If an 8 bit is not sensed, Counter 1 will remain on and inhibit the ready light.

#### Across the Tape

CE AID functions the same to pick the CC magnet and inhibit stepping.

If the 4 bit is not sensed before the end of MP 5 time, Decode 1 and Decode 2 will both be set. Decode 2 is set by CE AID, —Decode 1 and the positive shift of —MP 5. Decode 1 is set by CE AID, CB 8 and the positive shift of —MP 5.

If a bit is sensed between the end of MP 5 and the beginning

of MP 6, then Decode 1 will be reset by CB 8, Read Amp and Decode 2 being true.

At MP 6 time, Line Return 1 is set by MP 6, CE AID and Decode 2. Decode 2 is then reset by CE AID and the positive shift of —MP 6.

If the 5 bit is not sensed after the end of MP 6, then both the error and the ready lights will glow at 144 Deg. The lights will glow because CE AID, —CB 8 and —Decode 1 are true. This indicates correct head alignment.

If the 4 bit is read early, Decode 1 will be set before MP 5 time by Read Amp, CB 8 and —Decode 2. At 144 Deg. the error light will glow because —CB 8, CE AID and —Line Return 1 are true.

If the 5 bit is read late, after the end of MP 6, only the Ready light will glow, CB 8, Read Amp and —Decode 2 reset Decode 1. CB 8, Read Amp and CE AID generate a Counter Reset. At 144 Deg. —CB 8, CE AID and —Counter 1 are ANDED to turn on the Ready Light.



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## SEQUENCE OF EVENTS

### MT COUNTER

Set  $\phi$  conditions the counter to  $\phi$  count (All Counter Reset Except D). The normal stepping of the counters during a reader cycle is caused by emitter pulses, therefore, it is counting emitter pulses. [A read operation only uses ten (10) emitters.]

1. MP 1 = MT CTR A Sets & MT CTR D Resets
2. MP 2 = MT CTR B Sets
3. MP 3 = MT CTR A Resets & MT CTR C Sets
4. MP 4 = MT CTR B Resets
5. MP 5 = MT CTR A Sets & MT CTR D Sets
6. MP 6 = MT CTR B Sets
7. MP 7 = MT CTR A Resets, MT CTR C Resets & MT CTR E Sets
8. MP 8 = MT CTR B Resets
9. MP 9 = MT CTR A Sets & MT CTR D Resets
10. MP 10 = MT CTR B Sets

Note: This is how the machine sequentially steps to ten (10) count. In a normal read operation it would be taken back to  $\phi$  count to start the next cycle.

Under normal machine operation the counter is immediately conditioned to counts of  $\phi$ , 13, 14, & 15. IT DOES NOT STEP TO THESE COUNTS.

### READ OPERATION

1. Set Zero
2. Counter to Zero
3. CY. CL. Picks
4. MP 1 = Count One
5. MT/ST 1 Bit = MT Bit
6. MT Bit & Count One = D. L. 1 Sets
7. MP 2 = Count 2
8. MT/ST 2 Bit = MT Bit
9. MT Bit & Count 2 = D. L. 2 Sets
- NOTE: This is continued until MP 10 is coupled
10. MP 10 = 10 Count
11. X, Y, Z Parity check for Odd or -Odd
12. \*Odd & 10 Count = Increment Sets
13. Increment = Step Tape
14. End of Cycle = 10 Count & Character Code in the Data Latches

\* -Odd = Don't step the Tape & turn on Error Light.

### LOAD OPERATION

1. Push Keybutton
2. Set 15
3. 15 Count
4. LOAD SCH Shaft moves
5. Detent out & SCH Shoe on SCH Spring Clutch
6. Tape Movement
7. Sense Rewind Slot
8. Drop Detent & Tape Stops
9. Mt Read Sets
10. Set Zero
11. Load SCH Shaft Restores
12. Pick CY. CL. & Step Tape
13. Out of Rewind Slot
14. Steps until a "Good Feed Code (3 Bit, & -6 Bit) is read
15. MT Read resets when 3 Bit & -6 Bit is read
16. End of last cycle = 10 Count & Feed Code in Data Latches

### SEARCH RIGHT STATION

1. Push Search Keybutton
2. Set 14 = 14 Count
3. Set Transfer SCH STA if Left Tape is loaded
4. Search Signal Comes up
5. Cycle Console & Latch Head out
6. Load SCH Shaft moves
7. Let Search Key up
8. Detent out & Search Shoe on SCH Spring Clutch
9. Tape moves with Pressure Pad up
10. Sense Bit in Center Channel
11. MT Read Sets
12. Drop Detent & Tape Stops
13. Pick SCH. POS. MAG. & Head goes Home
14. Set Zero = Counter to Zero = Drop 14 Count
15. Search Signal goes Down
16. Load SCH Shaft Restores
17. Pick CY. CL. & Step Tape
18. Steps until a "Good" 3 Bit & -6 Bit is read
19. MT Read Resets when 3 Bit & -6 Bit is read
20. End of last cycle = 10 Count & 3 Bit in Data Latch

SEARCH LEFT STATION

1. If Transfer SCH STA. is up = Left Pressure Pad up

2. Left P. P. UP = Right P. P. DOWN

3. Search Signal comes up

4. Reset Data Latch 3

5. Cycle Console and Latch Head Out

6. Load SCH Shaft moves

7. Detent OUT & SCH Shoe on SCH Spring Clutch

8. Tape moves with Pressure Pad up

9. Sense Bit in Center Channel

10. MT Read Sets
11. Drop Detent & Tape Stops

12. Transfer SCH. STA. Resets = Search Signal goes Down

13. Search Shaft Restores

14. Pick SCH. POS. MAG. & Head goes home

15. Set Zero = Counter to Zero (14 Count not used to Search Left STA.)

16. Pick CY. CL. & Step Tape

17. Steps Until a "Good" 3 Bit & -6 Bit is read

18. MT Read is reset when 3 Bit & -6 Bit is read

19. End of Last Cycle = 10 Count & 3 Bit in Data Latch

OUTPUT TO TRANSLATOR

ORDINARY CHARACTER

Begin with RDY↑, OIF↓, OIF\*↓, and BSY↓.

At 1-2 of an OUTPUT Program Step, TSLTR SEL is SET.

1. At 1-5 the OUTPUT LATCHES are RESET and then SET with the NEW CODE. This is completed by the END of 1-5, B5-8 time.

2. At 1-5, B13-16 = BSY↑ = RDY↓.

3. BSY & TSLTR SEL & -FN & -OIF = TSLTR PR↑.

4. TSLTR PR = PICK CY. CL. & SELECTION MAGNETS.

5. 0 Degrees of cycle.

6. 65 Degrees = OIF↑ = DROP CY CL & SELECTION MAGNETS.

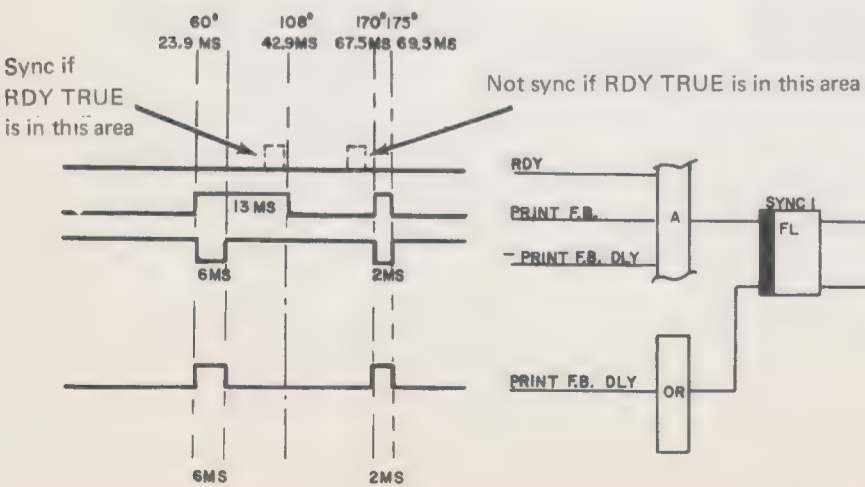
7. OIF = OIF\*↑ = BSY↓

8. 280 Degrees = OIF↓ = OIF\*↓.

9. -OIF\* & -BSY & BEG. P. S. = RDY↑.

10. RDY = CAN CHANGE THE CODE IN THE OUTPUT LATCHES.

NOTE: IF OUTPUT TO TSLTR P. S. occurs BEFORE RDY comes UP, -RDY & UPSET PRE INH = PRE INH↑ = INH↑ = WAITING.



SHIFT NOT MPX

SYNC OF SHIFT (INTERLOCK) (FN)	OUTPUT U. C.	LATCHES L. C.
	136	1346

Begin with RDY↑, OIF↓, OIF\*↓ AND BSY↓.

At 1-2 of an OUTPUT Program Step, TSLTR SEL is SET.

1. At 1-5 the OUTPUT LATCHES are RESET and then SET with the NEW CODE. This is completed by the end of 1-5, B 5-8 time.

2. TSLTR SEL & -OUT 2 & OUT 6 = FN↑.

3. FN & OUT 3 & BSY=TSLTR PR↑ = SHIFT (At 1-5, B 13-16 = BSY↑ = RDY↓) (BSY = CY. CL. PICKS)

4. 65 Degrees = OIF↑ = OIF\*↑ = BSY↓.

5. 65 Degrees & FN = DMY↑.

6. 280 Degrees & OIF = SYNC 2↑  
(280 Degrees does not = OIF↓ because -DMY↓ therefore RDY STAY<sup>c</sup> DOWN)

7. 280 Degrees & DMY & -DMY FN = TSLTR PR↑ = SHIFT 2ND CY.

8. 0 Degrees = 2ND CY.

9. 65 Degrees & SYNC 2 & DMY = DMY FN↑.

10. 280 Degrees does not = 3RD CY because -DMY FN↓.

11. 280 Degrees & DMY FN = OIF↓ = OIF\*↓.

12. -OIF = SYNC 2↓ & DMY↓.

13. -OIF\* & -BSY & BEG. P. S. = RDY↑.

14. RDY & UPSET PRE INH = DMY FN↓

## SHIFT MPX

Begin with RDY↑, OIF↓, OIF\*↓ AND BSY↓.

At 1-2 of an OUTPUT Program Step, TSLTR SEL is SET.

1. At 1-5 the OUTPUT LATCHES are RESET and then SET with the NEW CODE. This is completed by the end of 1-5, B 5-8 time.
2. TSLTR SEL & -OUT 2 & OUT 6 = FN↑.
3. FN & OUT 3 & BSY = TSLTR PR = SHIFT (At 1-5, B13-16 = BSY↑ = RDY↓) (BSY = PICK CY. CL.)
4. 65 Degrees = OIF↑ = OIF\*↑ = BSY↓.
5. 65 Degrees & FN = DMY↑.
6. 280 Degrees & OIF = SYNC 2↑.
- 7\* FN & OUT 3 & SYNC 2 & MPX = -OIF\*↑ (-OIF STAYS DOWN)
8. -OIF\* & -BSY = RDY↑ (MPX forces next character code into OUTPUT LATCHES)
9. 280 Degrees & DMY & -DMY FN = TRSTL PR↑ = character 2ND CY.
10. 0 Degrees = 2ND CY.
11. 65 Degrees & SYNC 2 & DMY = DMY FN↑.
12. 280 Degrees does not = 3RD CY. because -DMY FN↓.
13. 280 Degrees & DMY FN = OIF↓.
14. -OIF & DMY FN & -FN (character in OUTPUT LATCHES) = SYNC 1↑.
15. -OIF = SYNC 2↓ & DMY↓.
16. -OIF\* & -BSY & BEG P. S. = RDY↑.
17. RDY & UPSET PRE INH = DMY FN↓.

### NOTES:

- 7\* OIF\* will SET again as soon as its RESET is lost by FN becoming a character. This happens in STEP 9.  
The busy F. L. will SET at 1-5, B 13-16 to RESET RDY, then at the next Central B. T., after OIF\* SETS, BSY will RESET.

## FN OTHER THAN SHIFT

MPX OR -MPX	OUTPUT	LATCHES
	TAB C. R.	B. S.
	46 6	146

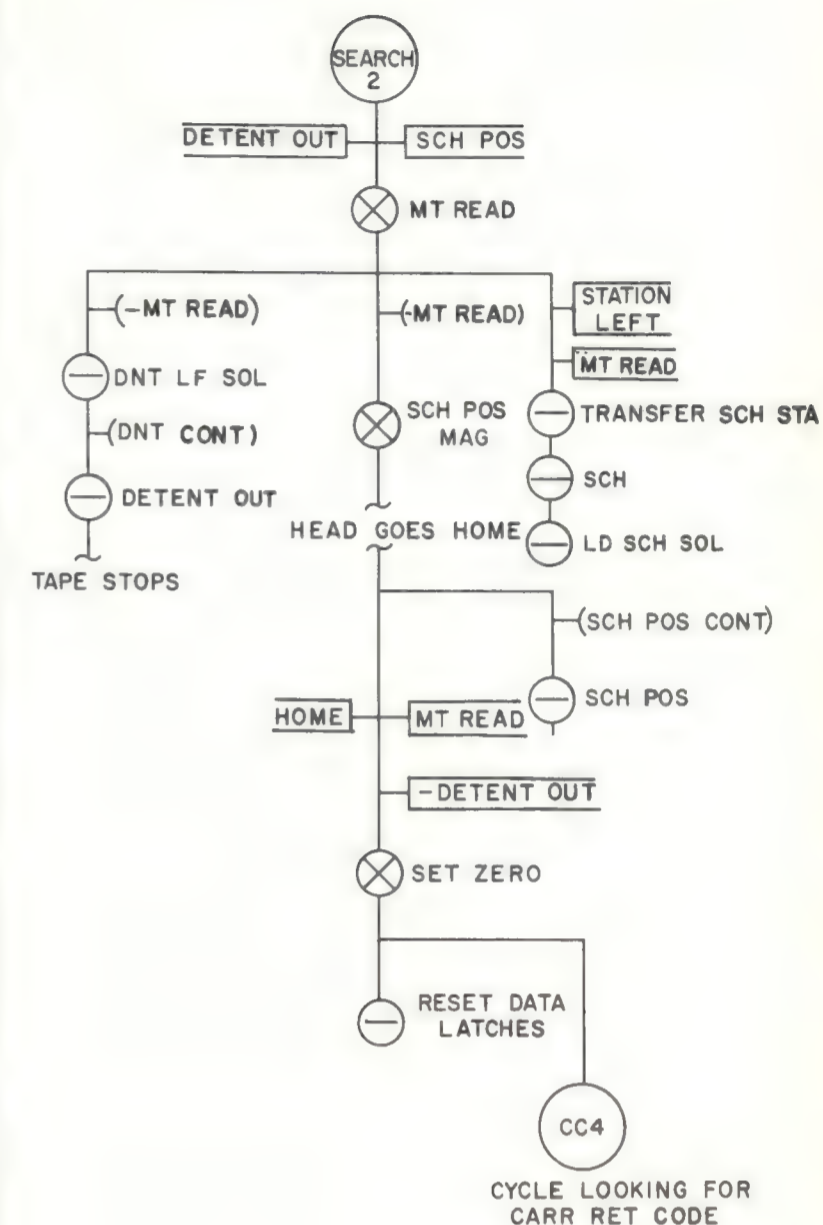
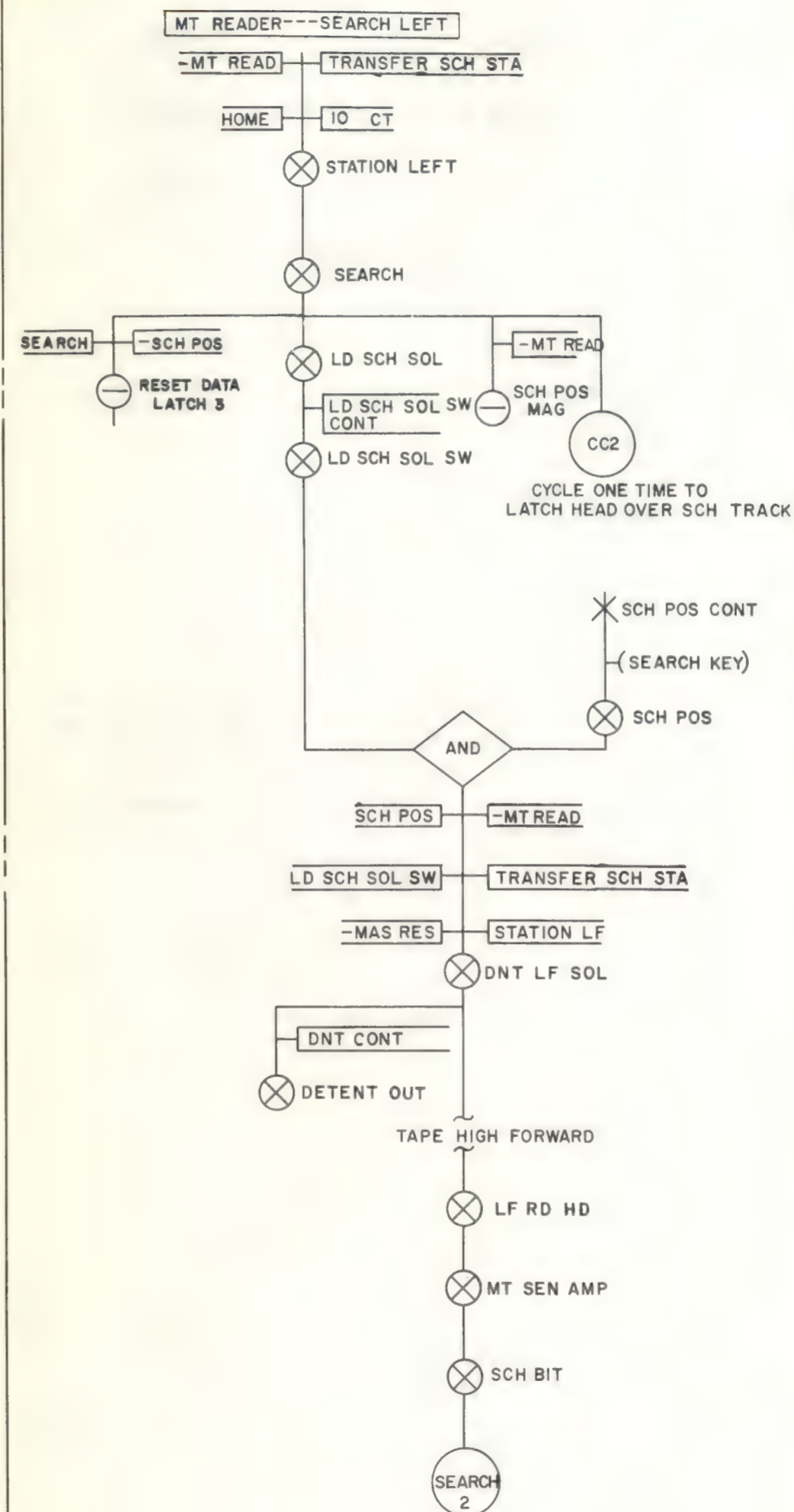
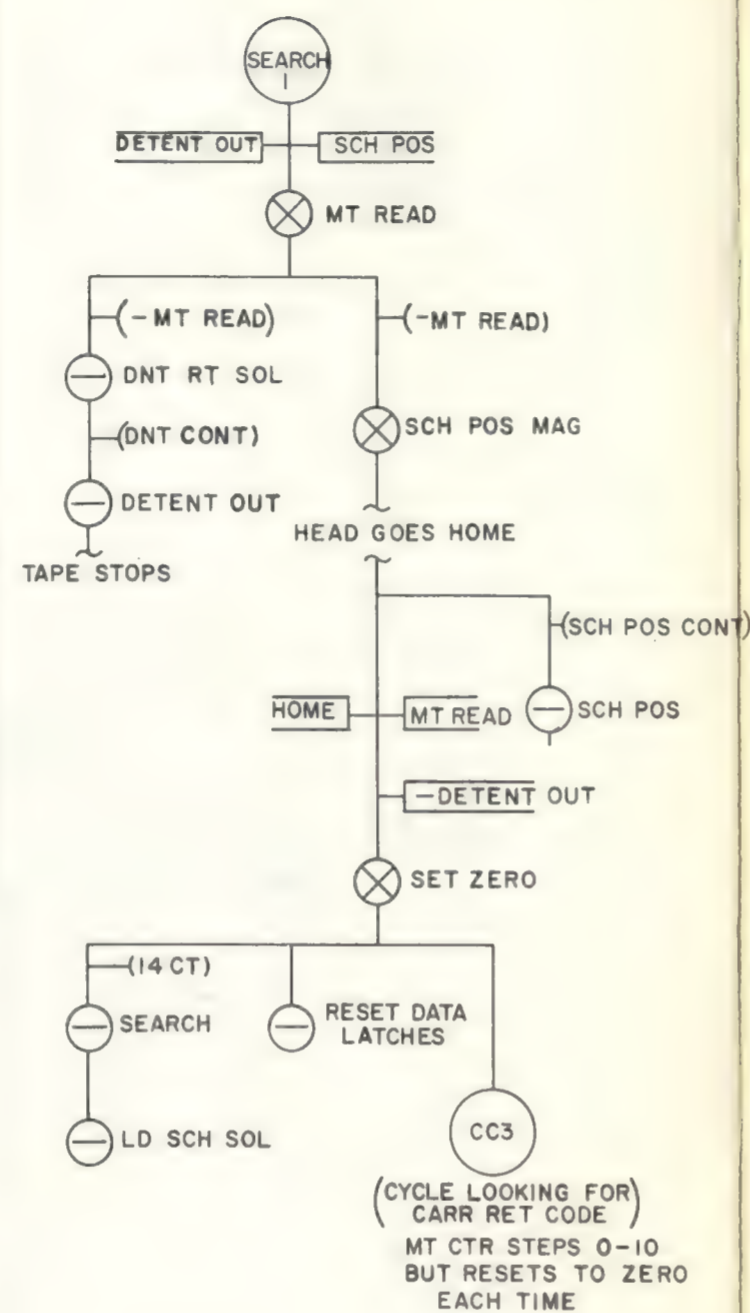
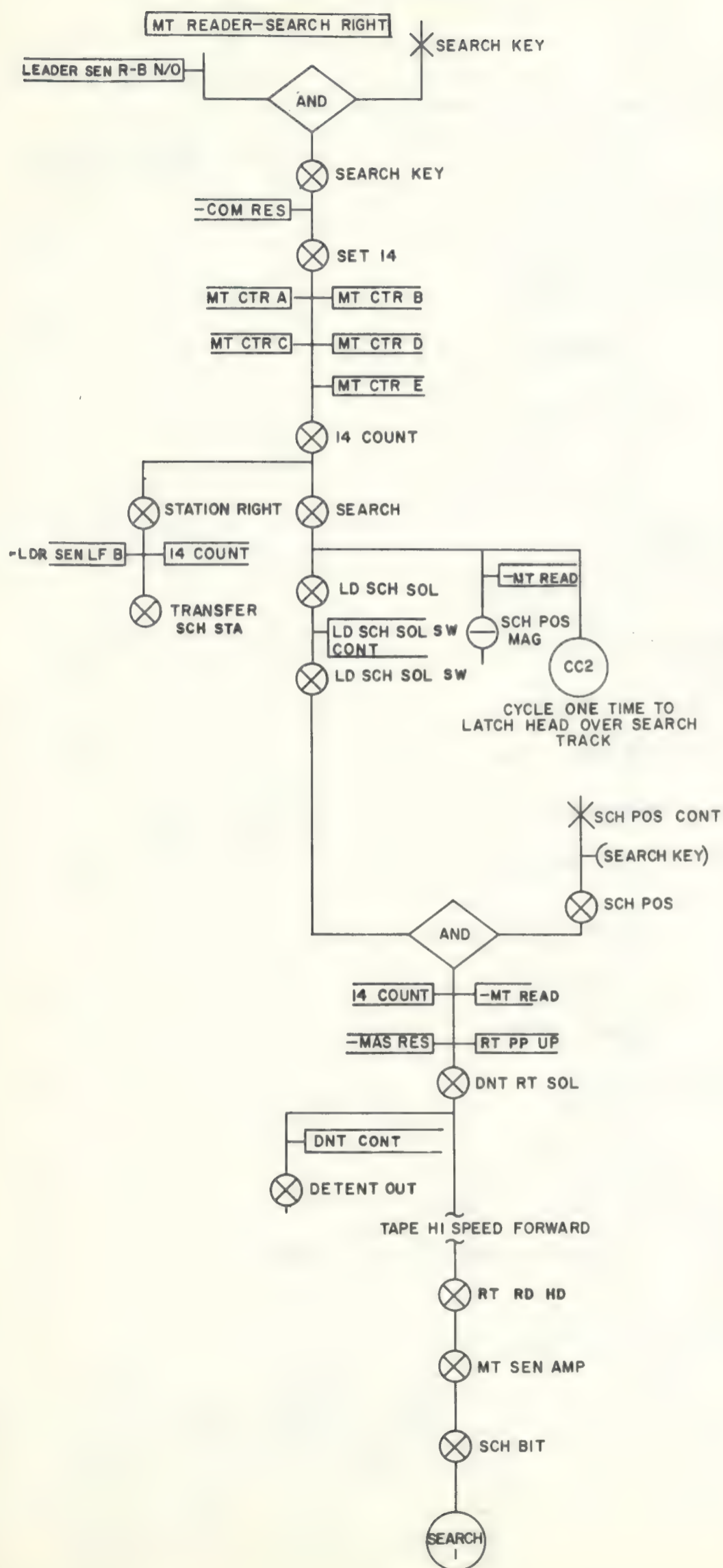
Begin with RDY↑, OIF↓ OIF\*↓ AND BSY↓.

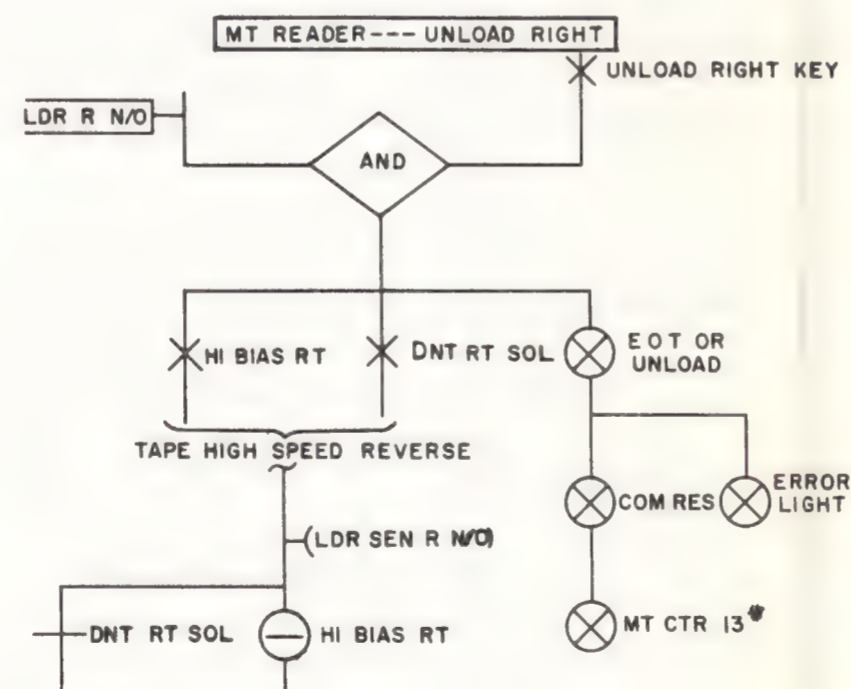
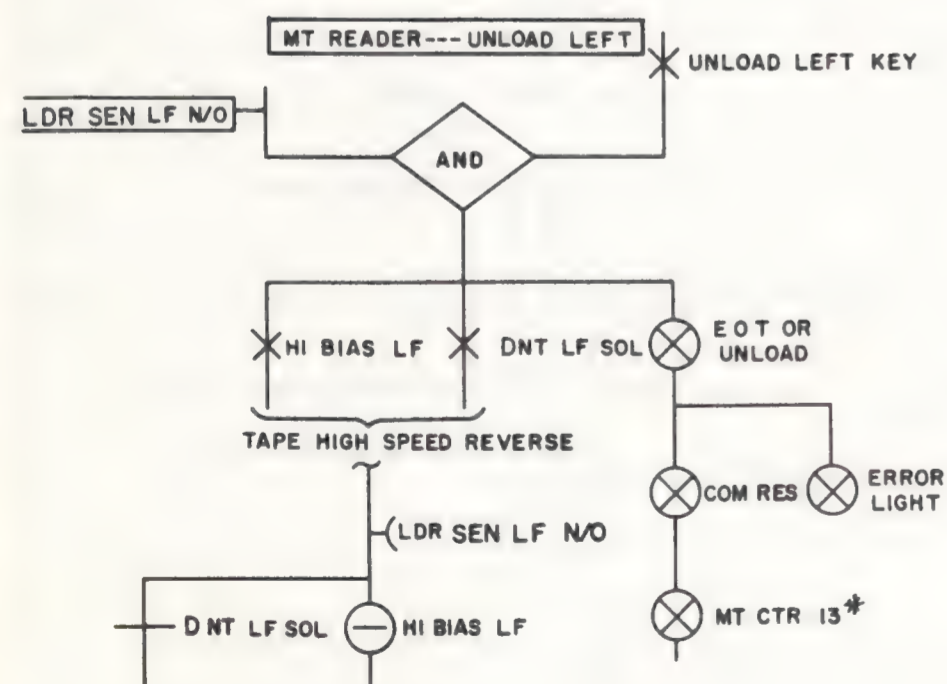
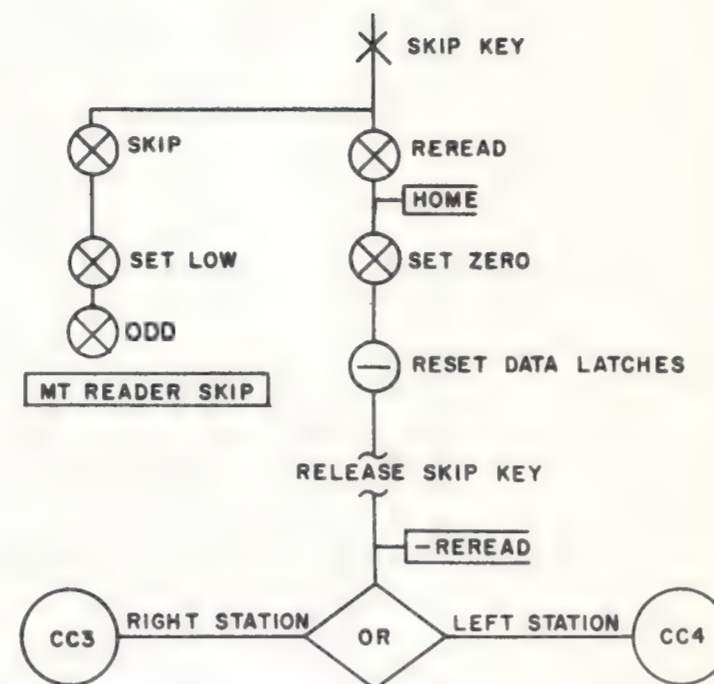
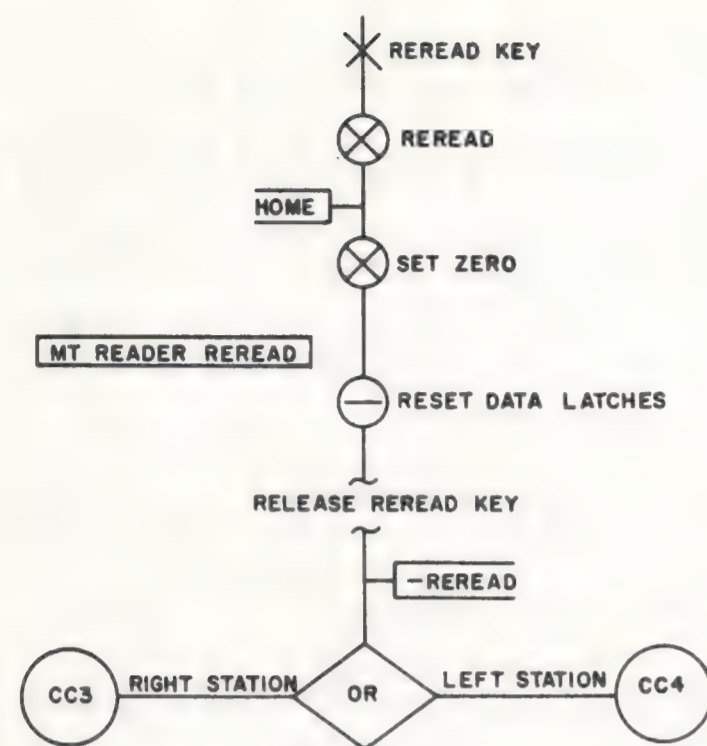
At 1-2 of an OUTPUT Program Step, TSLTR SEL is SET.

1. At 1-5 the OUTPUT LATCHES are RESET and then SET with the NEW CODE. This is completed by the end of 1-5, B 5-8 time.
2. TSLTR SEL & -OUT 2 & OUT 6 = FN↑.
3. FN & BSY & TSLTR SEL & -OIF = TSLTR CY. CL. (not selection magnets)
4. 65 Degrees = OIF↑ = OIF\*↑ = BSY↓.
5. 65 Degrees & FN (in the OUTPUT LATCHES) = DMY↑.
6. 280 Degrees & OIF = SYNC 2↑  
(280 Degrees does not = OIF↓ because -DMY↓ therefore RDY STAYS DOWN)
7. 280 Degrees & DMY & -DMY FN = TRSLTR PR↑ = TAB or C. R. 2ND CY.
8. 0 Degrees = 2ND CY. TAB or C. R.
9. 65 Degrees & SYNC 2 & DMY = DMY FN↑.
10. 280 Degrees does not = 3RD CY. because -DMY FN↓.
11. 280 Degrees & DMY FN & TAB + CR = TAB + CR SS for 165 M. S. (OIF can't RESET) Comp. carrier movement & TAB + CR then takes over and prevents OIF from RESETTING until the carrier stops.
12. Carrier stops and OIF RESETS = OIF\*↓.
13. -OIF = SYNC 2↓ & DMY↓.
14. -OIF\* & -BSY & BEG P. S. = RDY↑.
15. RDY & UPSET PRE INH = DMY FN↓

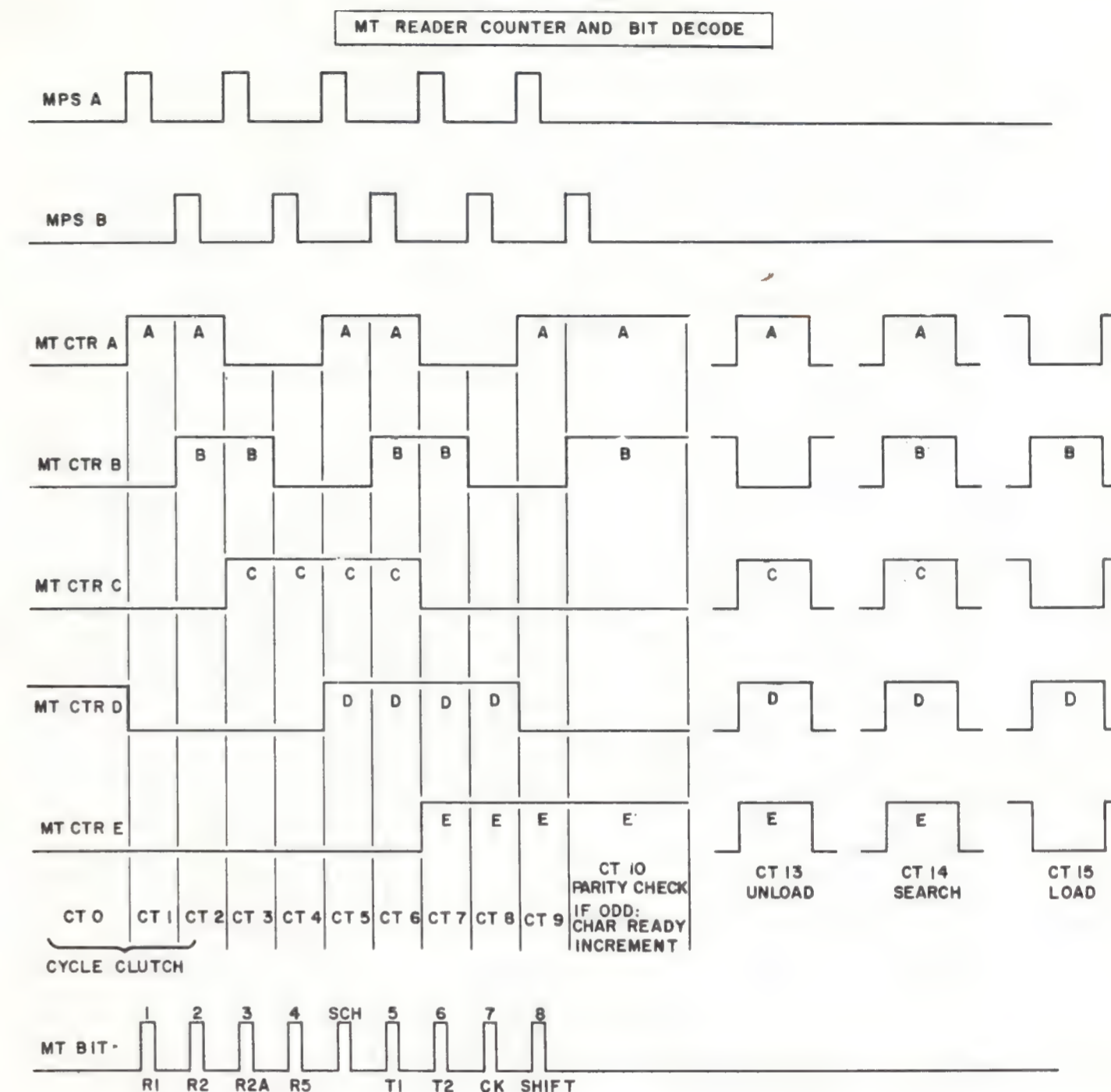








\*not required for the proper operation of unload.  
used so the counter won't be at any other count.



SCH	SH	R2A	R1	T2	T1	R2	R5
SCH	8	3	1	6	5	2	4
128	64	32	16	8	4	2	1
8	7	3	1	6	5	2	4
8	7	6	5	4	3	2	1
4	3	2	1	4	3	2	1
**	*	6	5	4	3	2	1
**	*	6	5	4	3	2	1

LATCHES  
MT/ST BITS  
BINARY BIT  
DATA LATCHES  
MT BITS  
P BUFFERS  
OUTPUT LATCH  
PERMUTATION BAR

\* the number 7 output latch and permutation bar are used only with press wire option for 4 unit escapement.

\*\* the number 8 output latch and permuntion bar are used for a no print operation.

REREAD, SKIP, UNLOAD LEFT AND RIGHT	
PAGE NO.0403	
IBM 6310/6320	

P ONLY CYCLE

P & Q CYCLE

SSA  
(K6D13)

SSB  
(K6B13)

A  
(G5D05)

B  
(G5B08)

TWR  
(G5B03)

P TIME  
(G6B11)

CEN BIT T  
(G5D11)

RESET BFR

-B AND -TWR  
(G5D10)

BMP STRB T  
(G6B02)

CURR SOURCE X  
LOG (G6D02)

CURR SOURCE Y  
LOG (G6D05)

REWO  
(D3D09)

ROWE  
(D3D05)

STR LTH STRB  
(G6B13)

STR BIT CTR A  
(COMP-G6D11)

STR BIT CTR B  
(COMP-G6B09)

RESET IND  
(F6D06)

LOAD IND  
(G5B11)

BIT T CTR A  
(G5D13)

BIT T CTR B  
(G6D06)

BIT 1-4  
(G5B10)

BIT 5-8  
(G6D10)

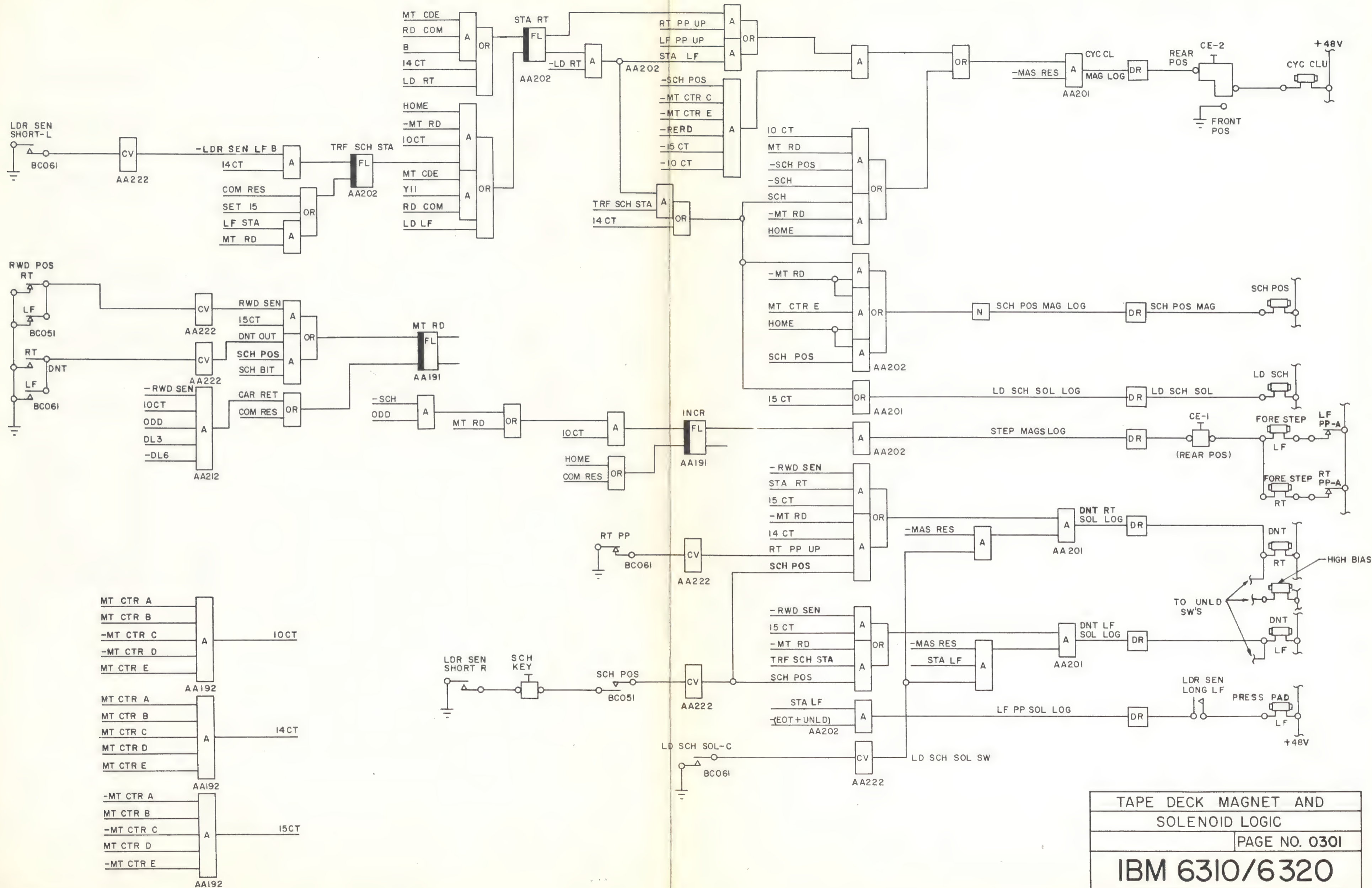
BIT 9-12  
(G5B12)

BIT 13-16  
(G6B12)

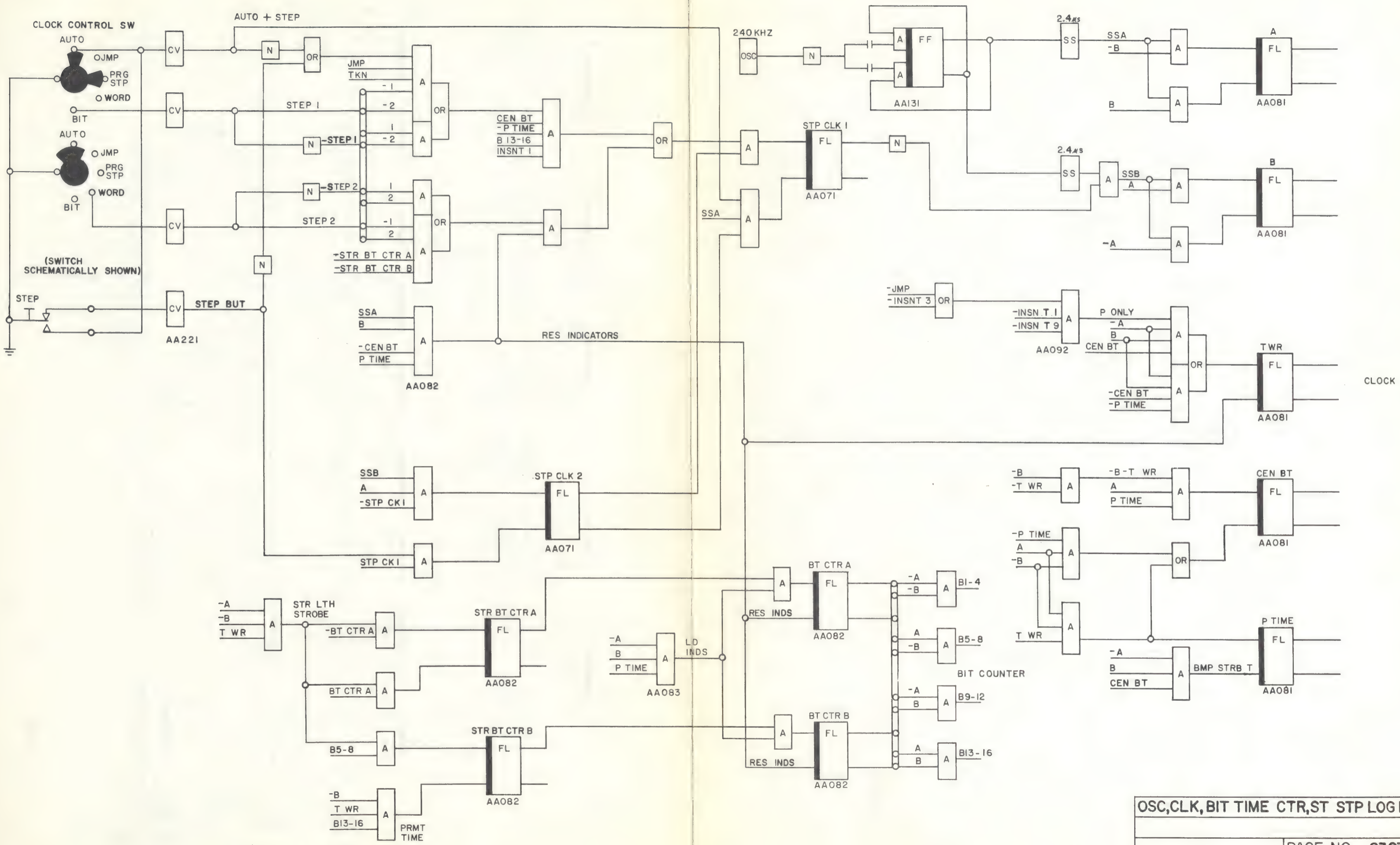
TIMING DIAGRAM BASIC  
CLOCK AND TIMING LOGIC  
PAGE NO. 0601

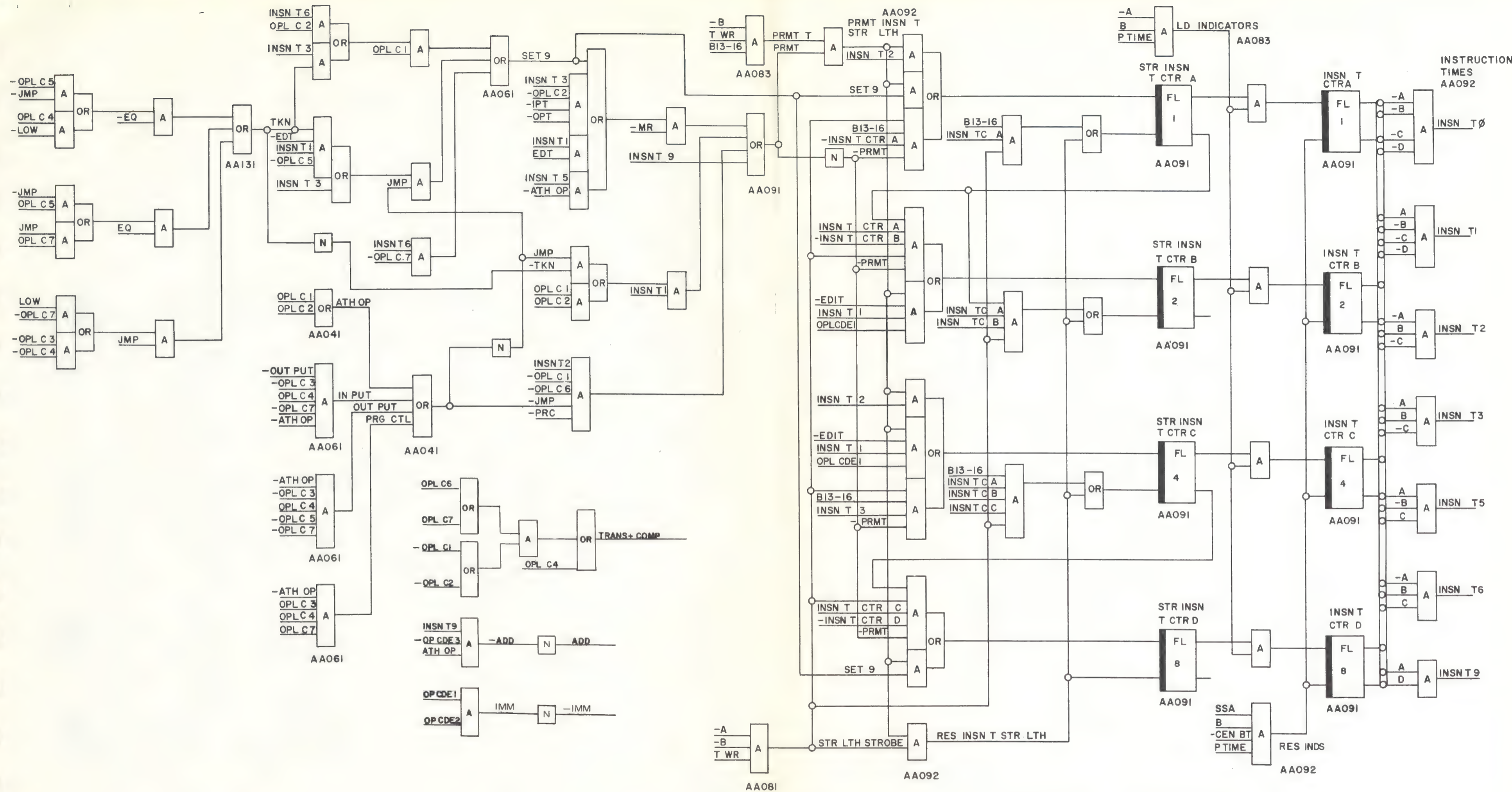
IBM 6310/6320

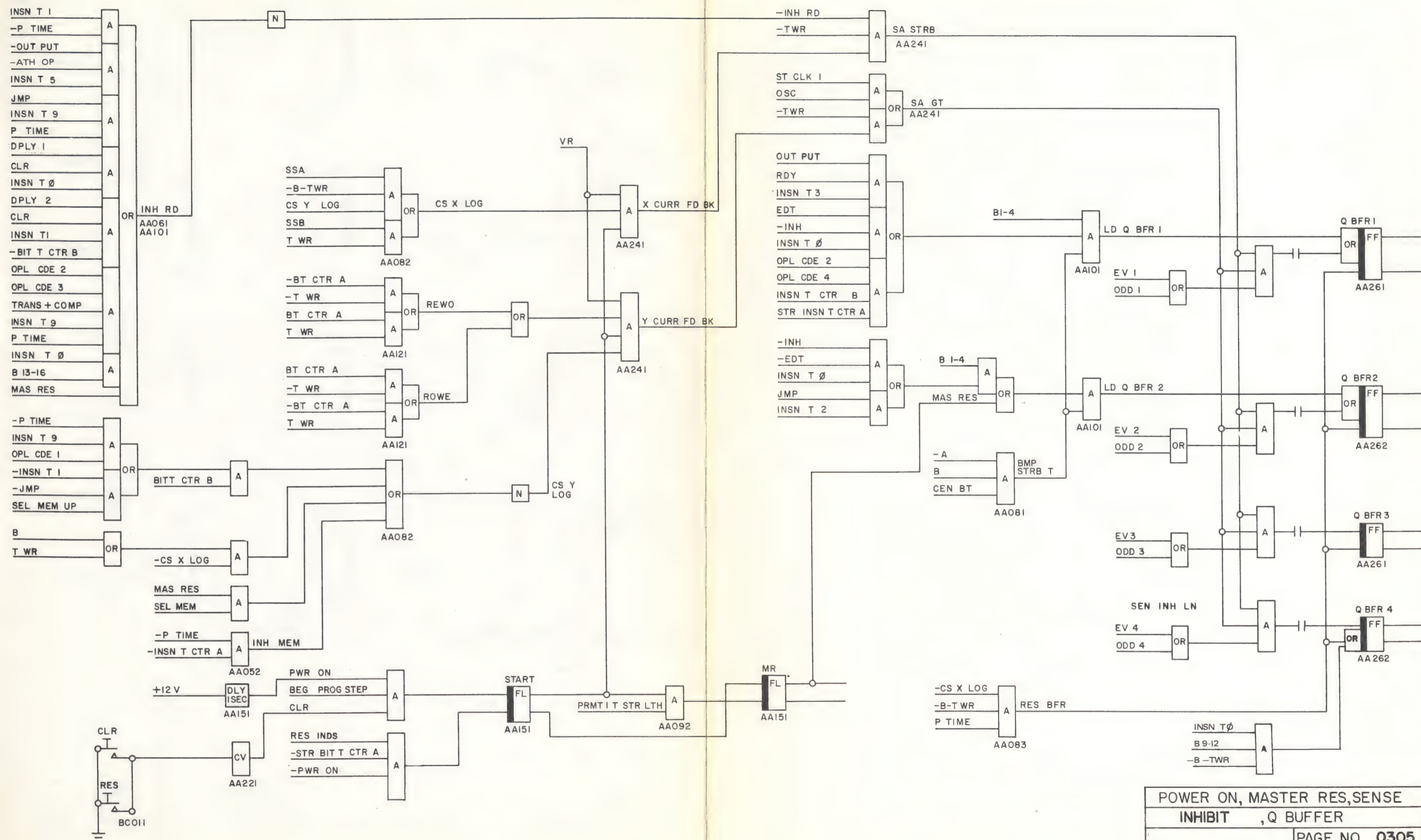


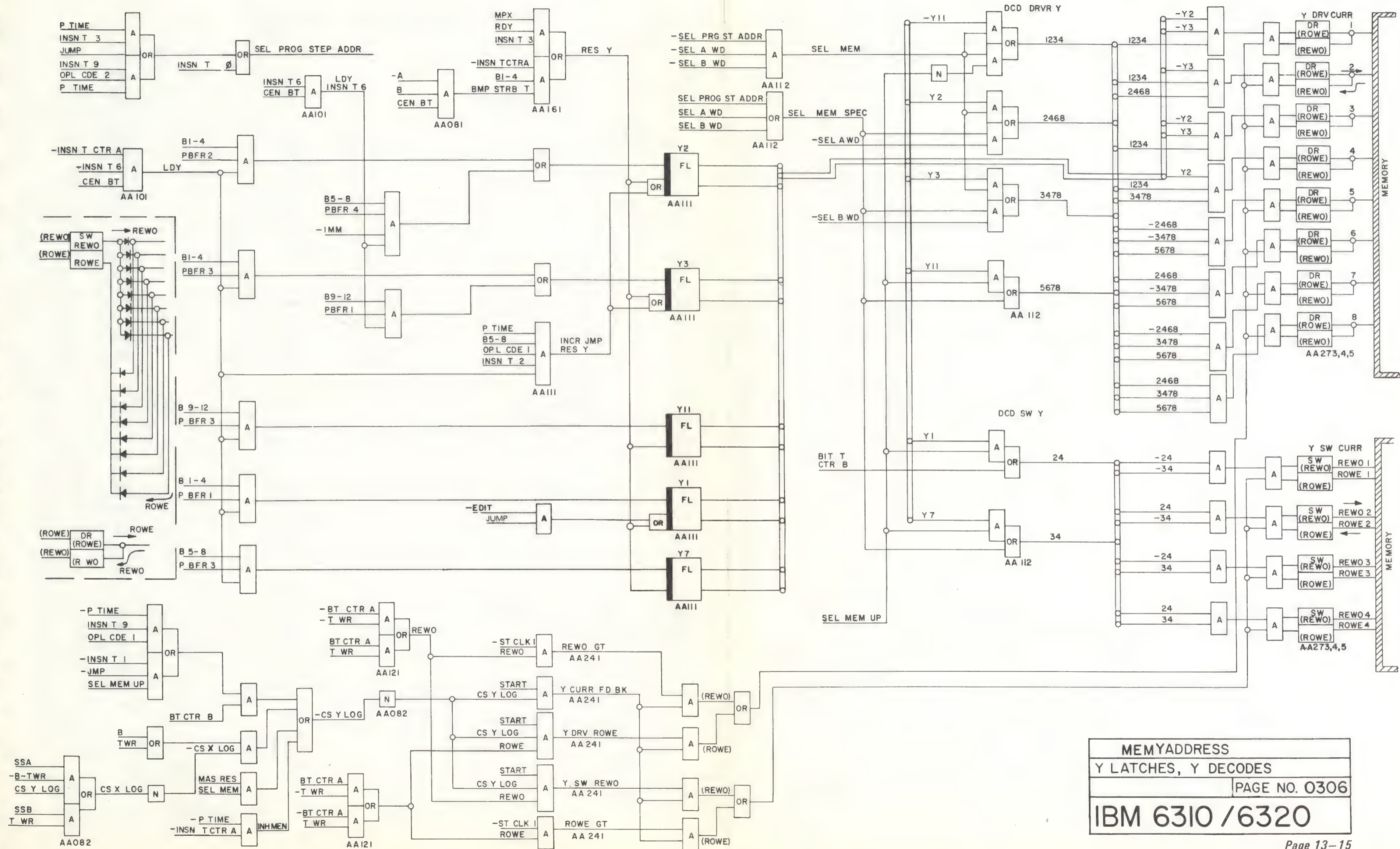


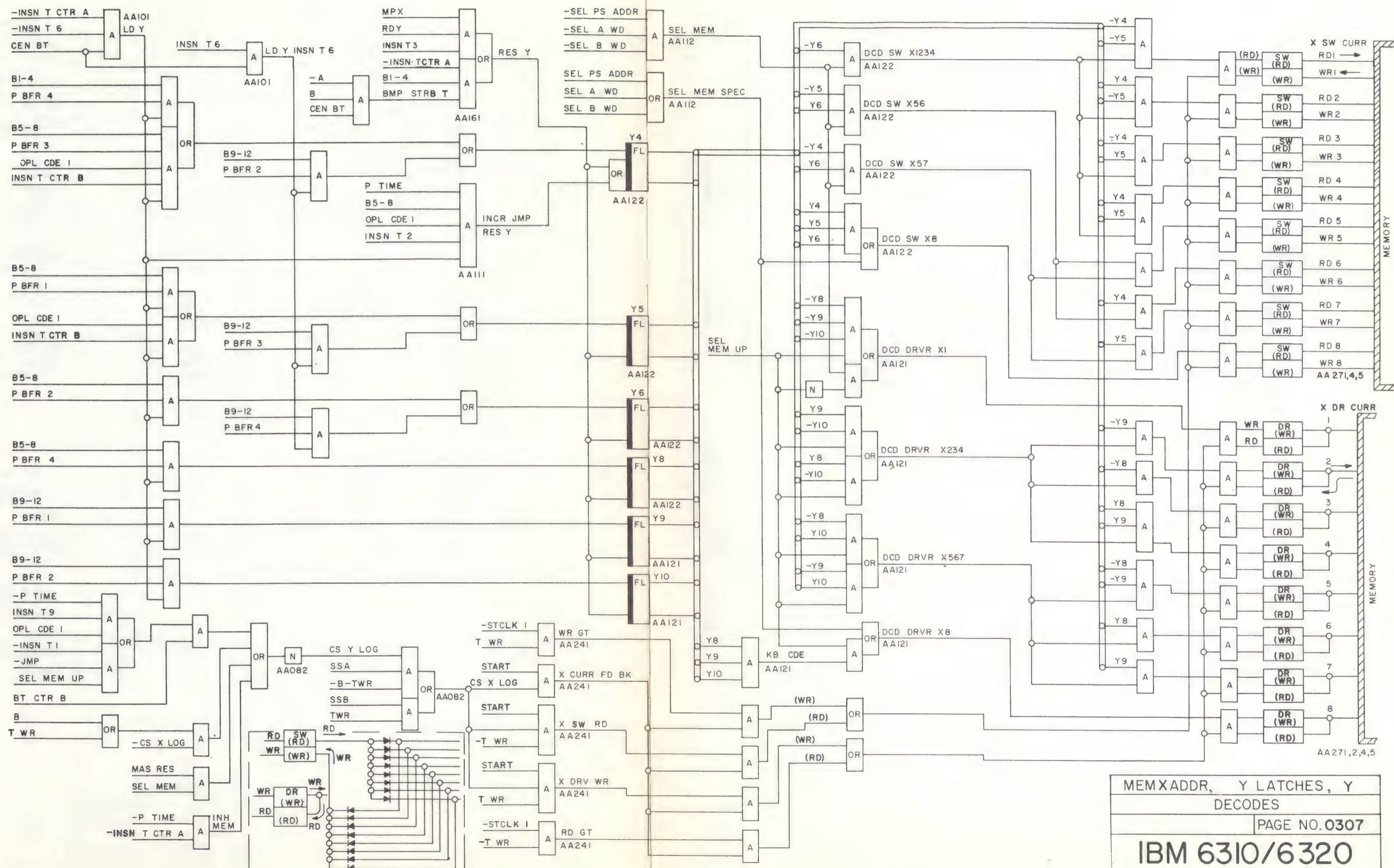




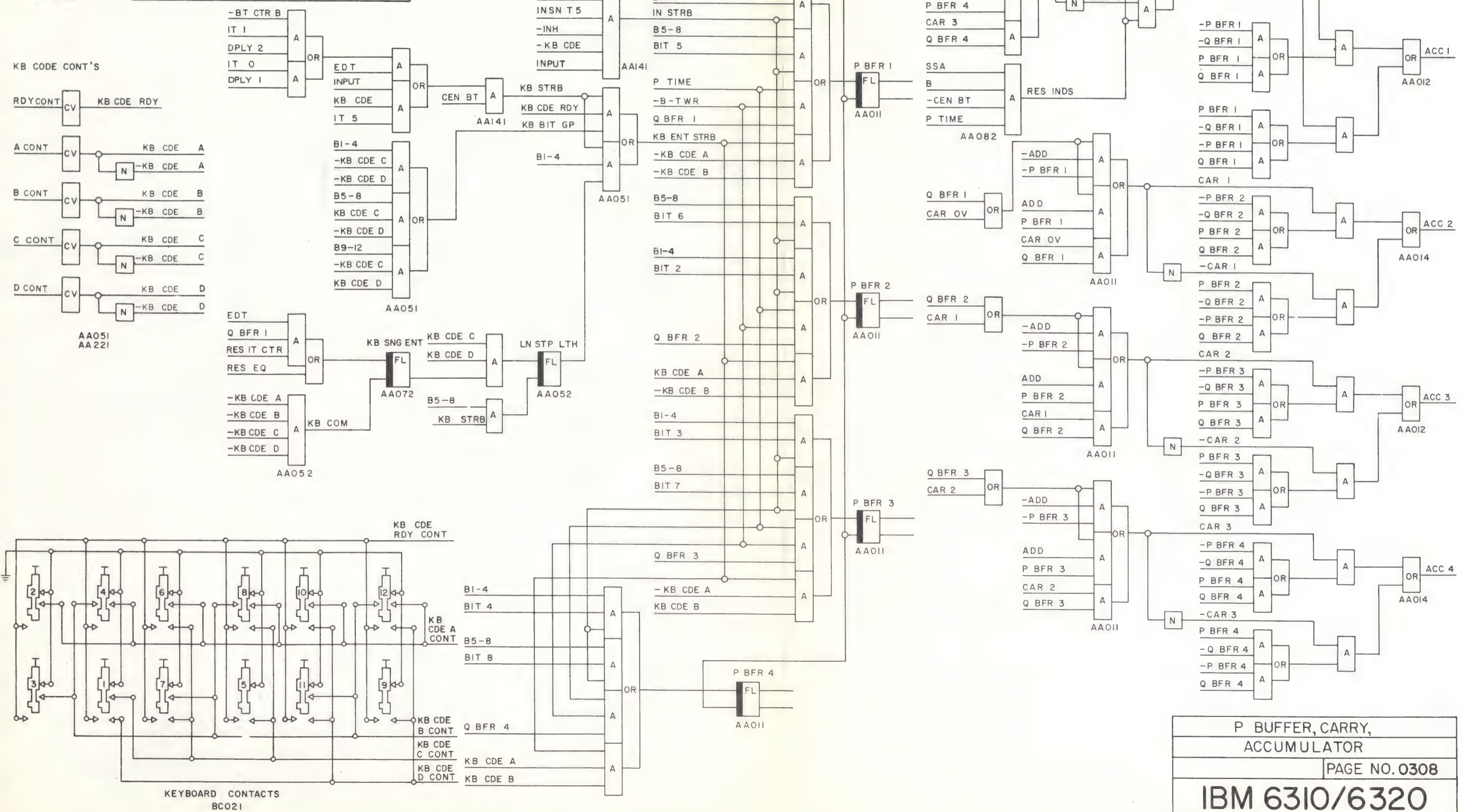


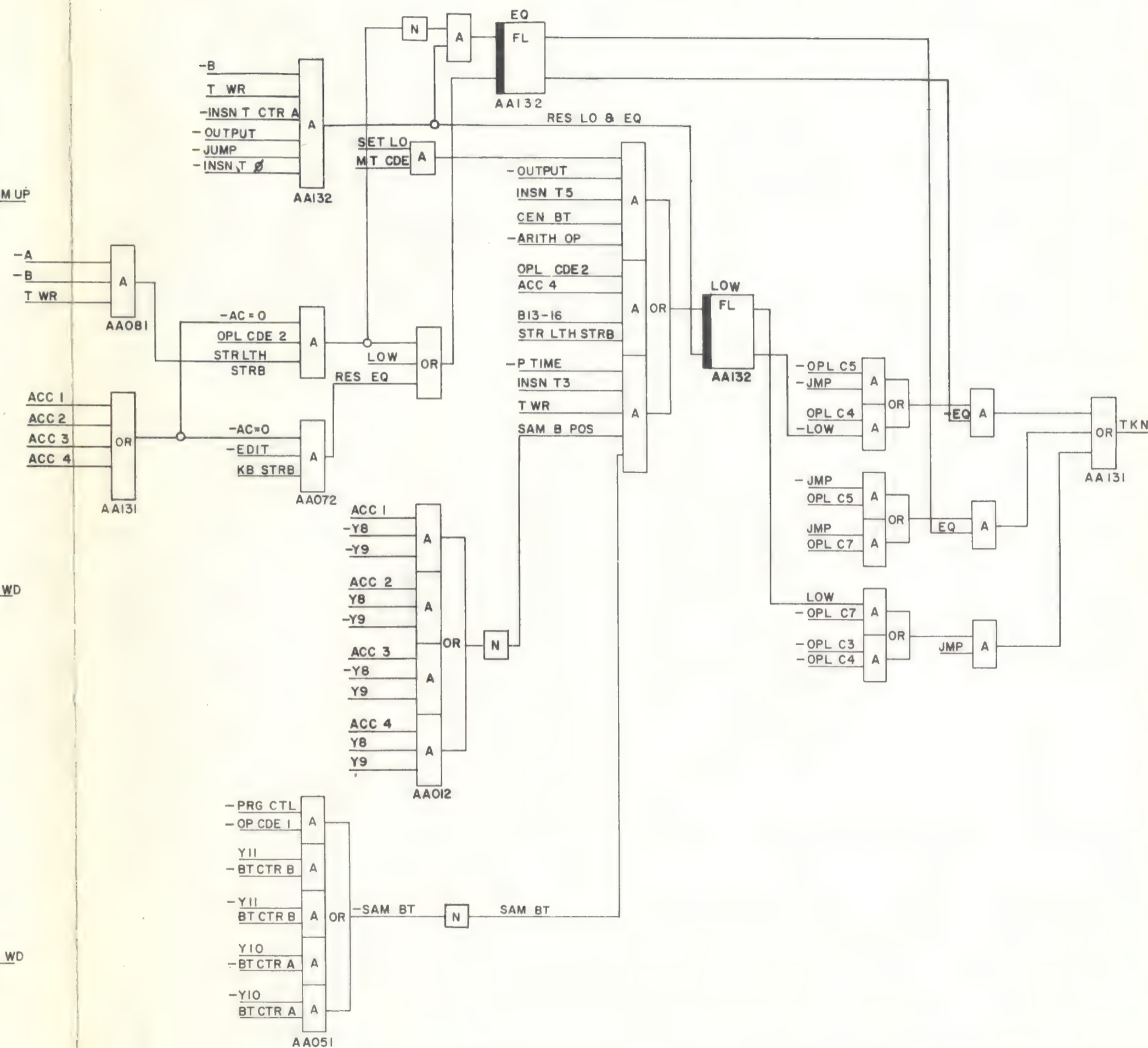
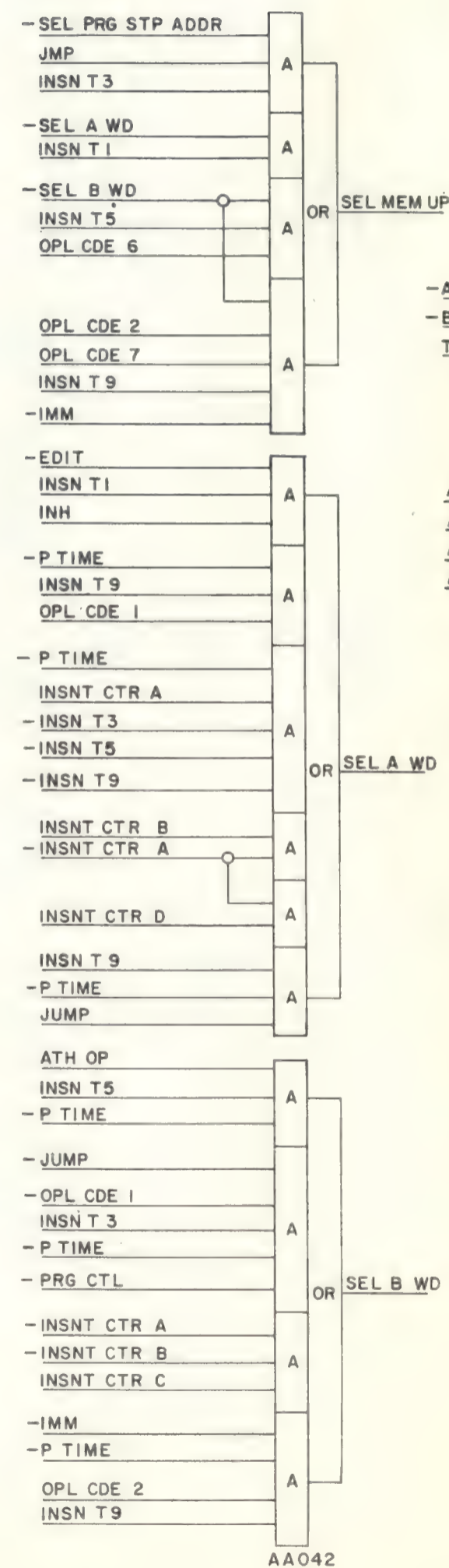
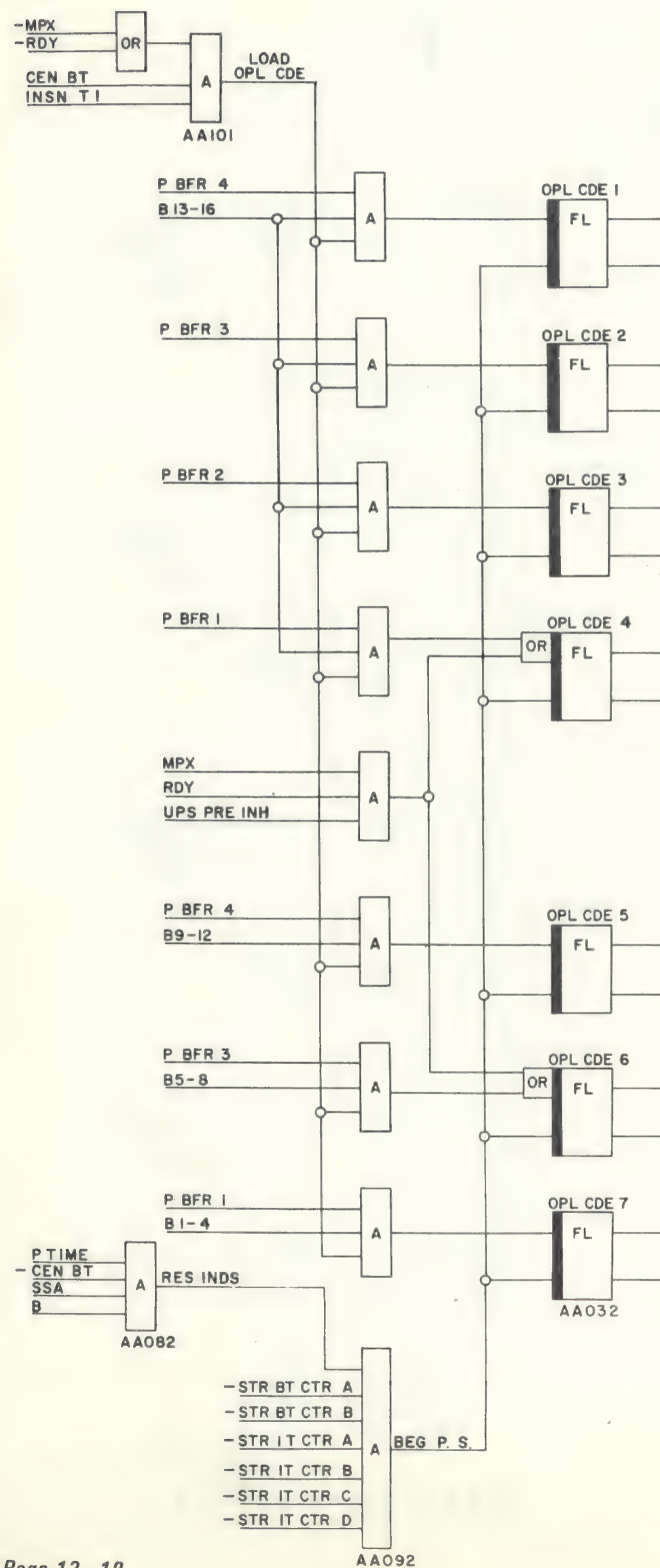




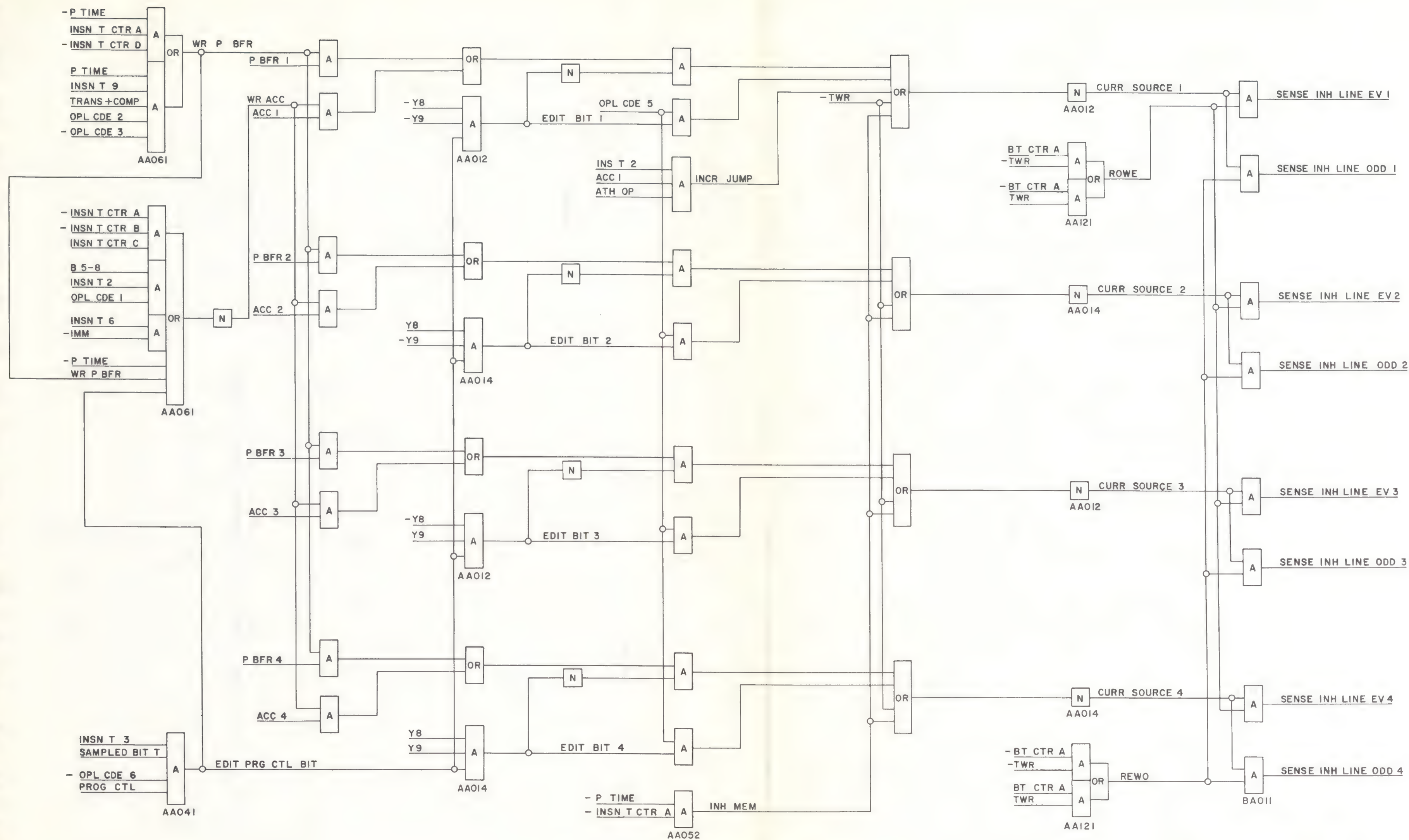


KEYBOARD CONTACT	12	11	10	9	8	7	6	5	4	3	2	1
KEYBUTTON	ST.	0	1	2	3	4	5	6	7	8	9	R
P BUFFERS	4	3	2	1	4	3	2	1	4	3	2	1
KEYBOARD CODE CONT.	A	B	A	D	A	B	A	C	A	B	A	-A B C D
BIT TIMES	9-12			5-8			1-4					

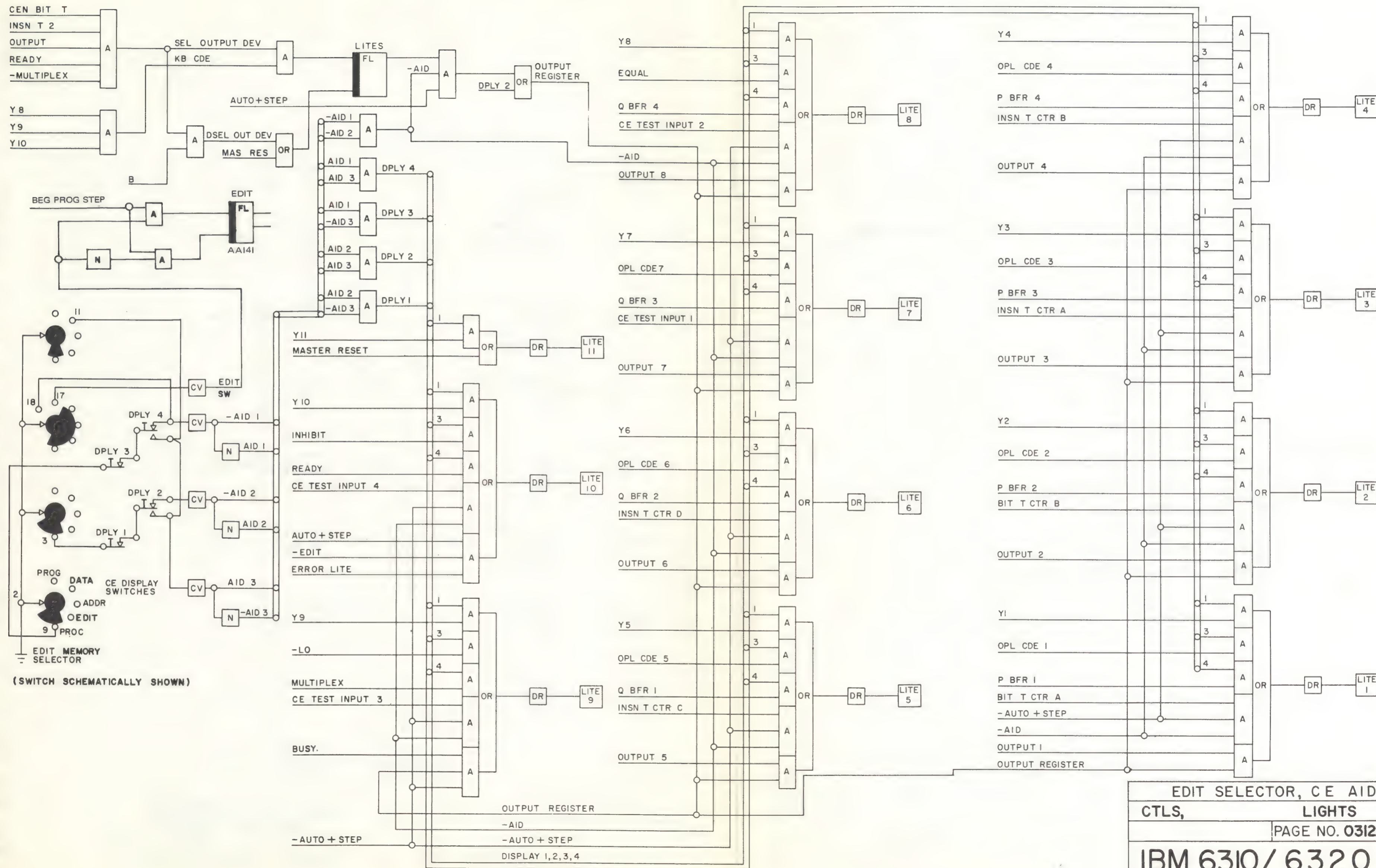


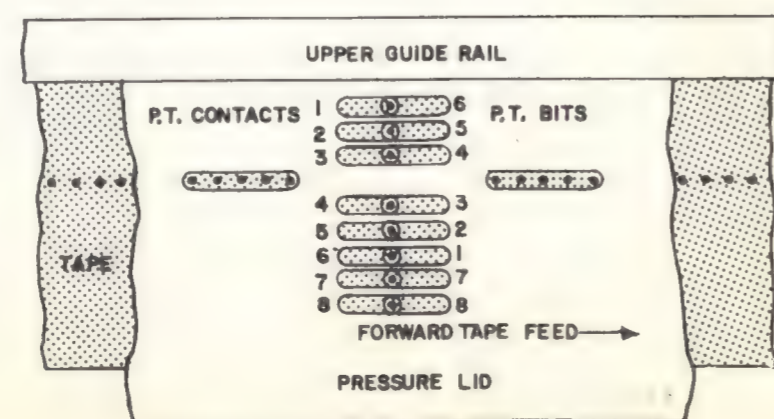
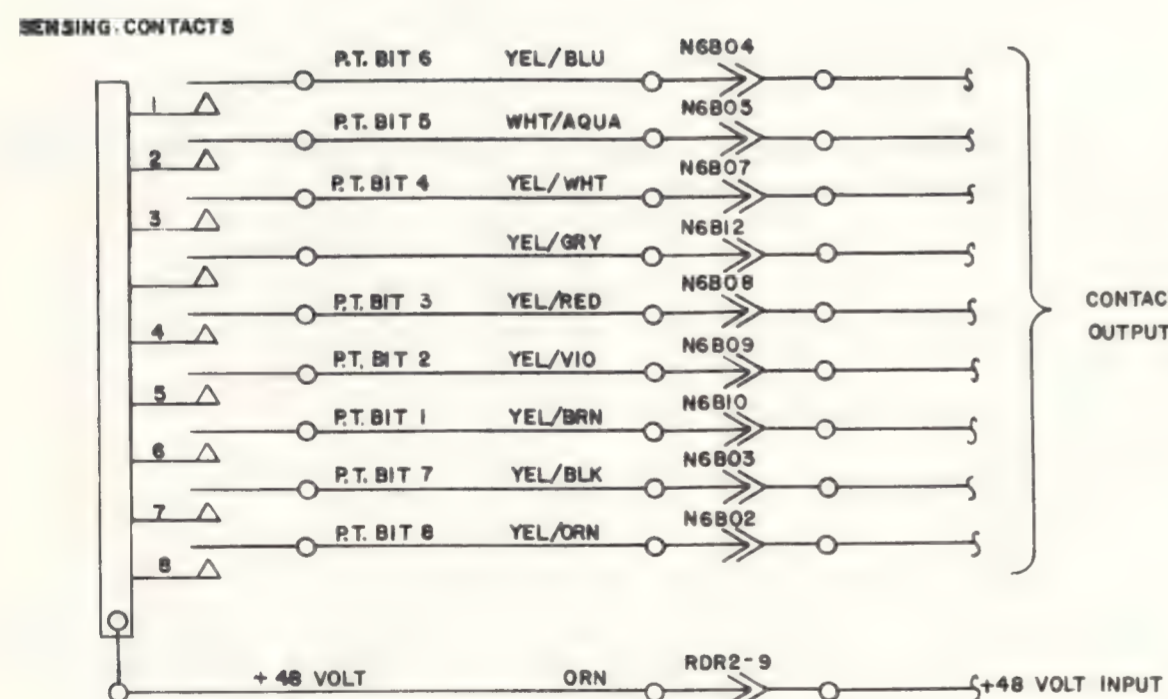
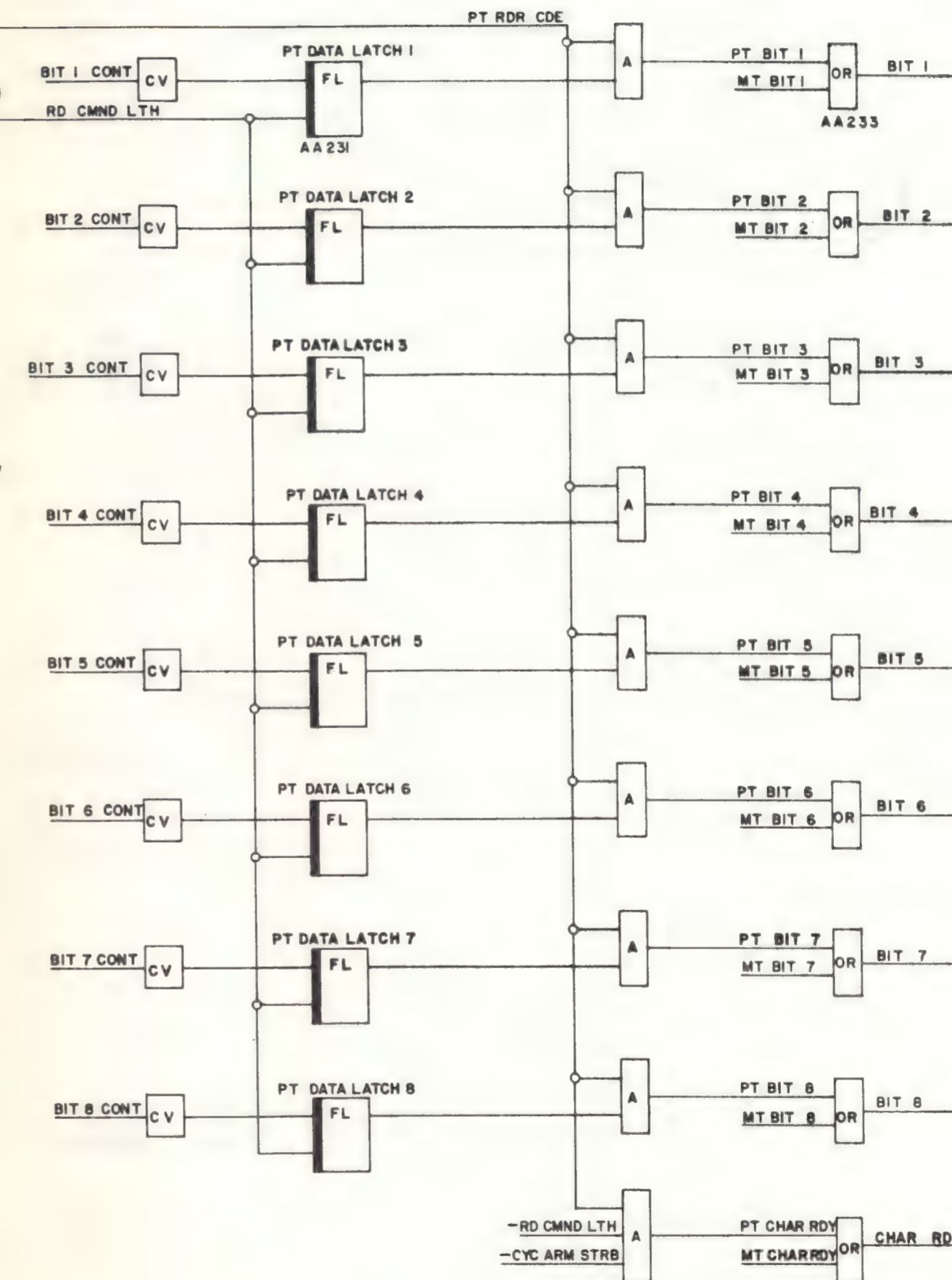
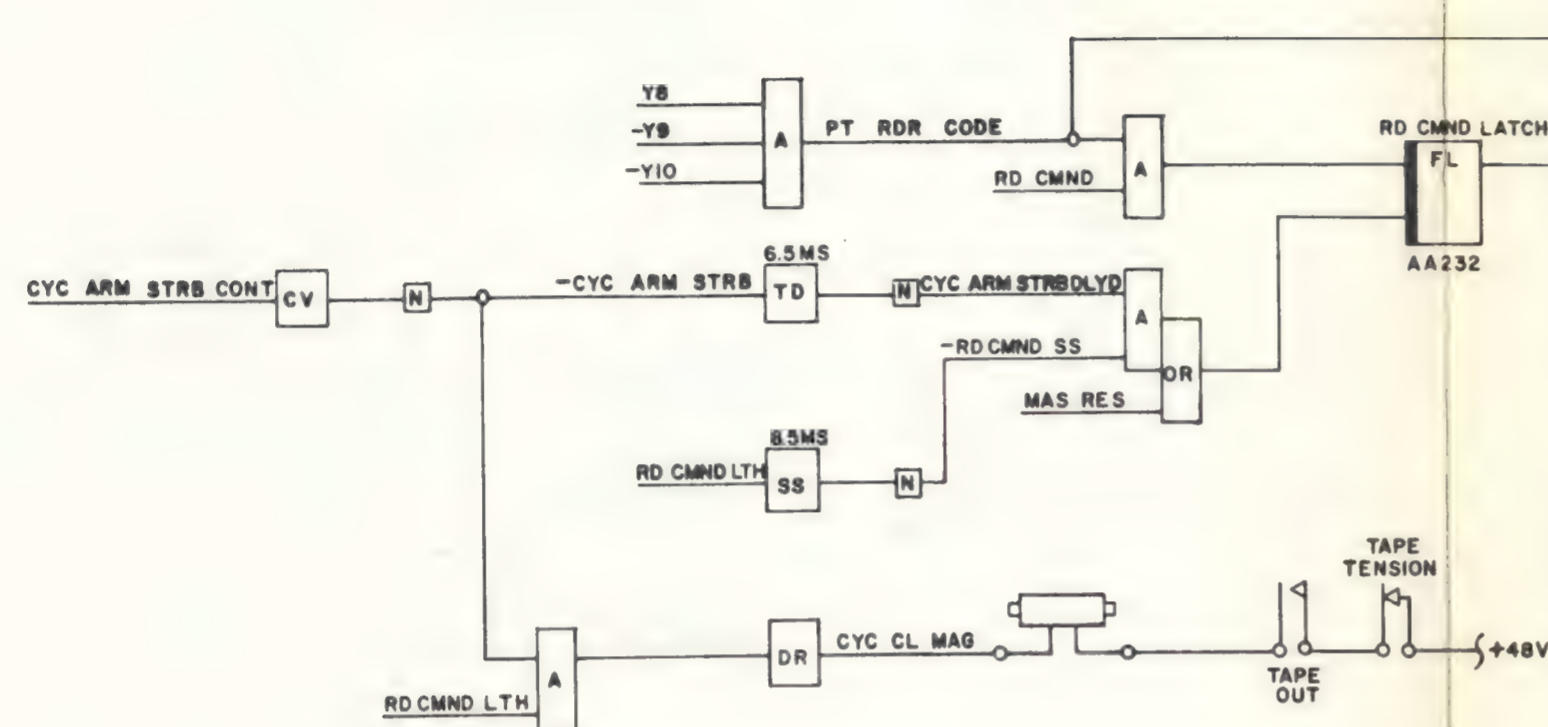


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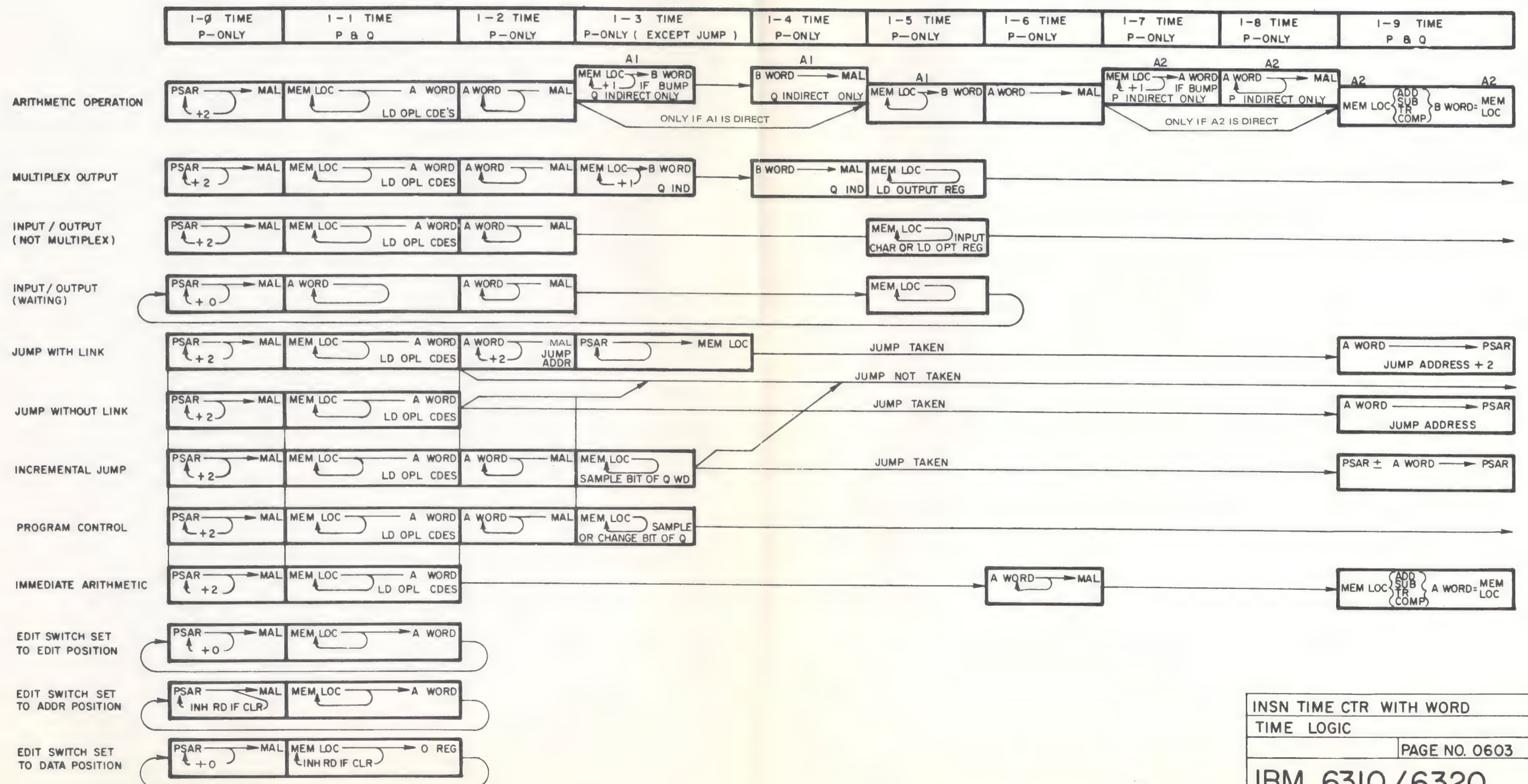






PAPER TAPE READER LOGIC  
AND TIMING DIAGRAM  
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# INSTRUCTION SET DATA FLOW







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MT/SR

ILD and Function Charts

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## SEQUENCE OF EVENTS

### MT/SR RECORD

1. Printer Cycles
2. Print the Character
3. Record 1 Sets
4. Transmit Contacts Sets Buffers
5. Pick Console CY. CL.
6. Fore Stroke
  - A. C. B. 8 Makes
  - B. MP 1 = Record 2 Sets
  - C. MP 2 = Record 1 Resets
  - D. MP 3 thru MP 11 = Write Bits
  - E. C. B. 8 Breaks
  - F. Record 2 Resets
  - G. Buffers Reset
7. Backstroke
  - A. MP 1 = Backstroke Sets & Counters Reset
  - B. Pick Forestep MAG.
  - C. Bits read on Backstroke Steps counter one On & Off
  - D. Parity Check & Step Tape.

### MT/SR ERROR CORRECT

1. Push B. S. Keybutton
2. Printer Back Spaces
3. Record 1 Sets
4. Transmit Contacts Sets Buffers
5. Pick Console CY. CL.
6. Forestroke
  - A. C. B. 8 Makes
  - B. Error Correct Sets = Error resets = Error light & Kbd lk off.
  - C. MP 1 = Record 2 Sets
  - D. MP 2 = Record 1 Resets
  - E. MP 3 thru MP 11 = Don't write or erase
  - F. C. B. 8 Breaks
  - G. Record 2 Resets
  - H. Buffers Reset
7. Backstroke
  - A. MP 1 = Backstroke Sets
  - B. Pick Backstep MAG.
  - C. Headslide Home
  - D. Back step Tape

### MT/SR LINE RETURN

1. Depress Line Return Key
2. Line Return 1 Sets
3. Hi bias SOL Picks
4. Console CY. CL. Picks
5. Forestroke
  - A. C. B. 8 Makes
  - B. C. B. 8 Breaks
  - C. Console CY. CL. Picks
6. Backstroke
  - A. MP 1 = Backstroke & Line Return 2 sets
  - B. Backstep MAG Picks
  - C. Backstep Tape
  - D. Headslide Home insures decode 1 is reset
7. Forestroke — of 2nd & Successive Cycles
  - A. C. B. 8 Makes & Home Sw Transfers
  - B. Reset to Decode 2 Removed & Decode 1 Removed
  - C. If a 1 or 2 Bit is read = Decode 1 Set = Decode 2 cannot set. Line return 1 cannot reset = CY. CL. will repick when C. B. 8 breaks
  - D. MP 3 = Decode 1 & Decode 2 sets if Item 7—C did not happen
  - E. If a 3 Bit is sensed after Item 7—D = Decode 1 resets
  - F. MP 4 always = A reset on Decode 2
  - G. Any Bit sensed after MP 4 will set Decode 1 if it is down. This will repick CY. CL. when C. B. 8 breaks.
  - H. MP 8, if decode 1 is down at this time, only a 3 Bit was read. (A 7 or 8 bit after MP 8 = 3, 7, 8 = U. C. CR.)
  - I. Decode 1 down = Line return 1 resets.
  - J. Line Return 1 down = Drop Hi bias, don't back step & don't pick the CY. CL. again.
  - K. Headslide Home = Line return 2 resets.

## MT/SR LOAD

1. Depress Load Key
2. Load Search Shaft Moves
3. Load 1 or Counter 16-45 Sets & Detent Sol. Picks.
4. Load Tape to B. O. T. Slot
5. Drop Detent & Tape Stops
6. Pressure Pad Sol Picks
7. Drop Load Search Sol
8. Load 2 or Counter 31-60 Sets
9. Console CY. CL. Picks
10. -C. B. 8 & Load 1 & Load 2 will repick the CY. CL. near the end of each forestroke until the B. O. T. roller comes out of the B. O. T. slot
11. Forestroke - First cycle after B. O. T. Slot
  - A. C. B. 8 Makes
  - B. MP 3 = Try to write a 1 Bit
  - C. MP 5 = Try to write a 3 Bit
  - D. MP 8 = Try to write a 5 Bit
  - E. C. B. 8 Breaks
  - F. Console CY. CL. Picks
12. Backstroke - First Cycle after B. O. T. Slot
  - A. MP 1 = Backstroke Sets & Counter Reset.
  - B. Pick Forestep MAG.
  - C. No Bits read on Backstroke = Counter one stays off
  - D. Step Tape
  - E. Head Slide Home = Load 1 or Counter 16-45 Resets

NOTE: On the second & successive cycles Item 11-F will be eliminated and the CY. CL. will not pick until Item 12-E when the head slide gets home. Load 1 (Item 12-E) will stay down after the first cycle out of the B. O. T. slot.

13. On any cycle after the first one out of the B. O. T. Slot if counter 1 is on when MP 11 is coupled on the backstroke; Load 2 or counter 31-60 will reset and the CY. CL. will not pick when the head slide gets home. Counter 1 being on indicates Odd Bit Parity.

## MT/SR

### RECORD PREFIX CODE

1. Depress Prefix Key.
2. \*Keyboard Lock SOL. Picks and Keyboard Mode contact opens
3. Prefix Record 1 and Record 1 Set
4. RED RIB. MAG. Picks
5. Buffers R1, R2A & R5 Set (Transmit Contacts)
6. Console CY. CL. Picks
7. Forestroke
  - A. C. B. 8 Makes
  - B. MP 1 = Record 2 Sets
  - C. MP 2 = Record 1 Resets
  - D. MP 3 Thru 11 = Write Bits
  - E. C. B. 8 Breaks
  - F. Record 2 Resets
  - G. Prefix Record 2 Sets
  - H. Buffers Reset
8. Backstroke (Same as Record, Item 7)

\*Keyboard unlocks when Prefix Button is released.

## MT/SR

### PRINT CHARACTER EXCEPT X FOLLOWING PREFIX CODE

NOTE: Prefix Record 1, Prefix Record 2 and Red Ribbon Magnet are still up Because of the Prefix Cycle.

1. Depress Key
2. Print the Character in Red
3. Prefix Record 1 Resets
4. Record 1 Sets
5. Transmit contacts Set Buffers
6. Pick Console CY. CL.
7. Forestroke
  - A. C. B. 8 Makes
  - B. MP 1 = Record 2 Sets, Prefix Record 2 Resets
  - C. Red Rib MAG. Drops
  - D. MP 2 = Record 1 Resets
  - E. MP 3 thru 11 = Write Bits
  - F. C. B. 8 Breaks
  - G. Record 2 Resets
  - H. Buffers Reset
8. Backstroke (Same as Record, Item 7)

# MT/SR

## X FOLLOWING PREFIX CODE

NOTE: Prefix Record 1, Prefix Record 2 and Red Ribbon are still up because of the Prefix Cycle.

1. Depress X Keybutton
2. Print the X in Red
3. Prefix Record 1 Resets
4. Record 1 Sets
5. Transmit Contacts = Buffers Set
6. Console CY. CL. Picks
7. Forestroke
  - A. C. B. 8 Makes
  - B. MP 1 = Record 2 Sets (Prefix Record 2 stays up)
  - C. MP 2 = Record 1 Resets
  - D. MP 3 thru MP 11 = Record an X
  - E. C. B. 8 Breaks
  - F. Record 2 Resets
  - G. Buffers Reset
8. Backstroke
  - A. MP 1 = Backstroke Flip Latch Sets & Counter Reset
  - B. Pick Forestep MAG.
  - C. Bits read on Backstroke Steps Counter One
  - D. Parity check & Step Tape
  - E. Headslide Home = Reference Flip Latch Sets (Odd or Even Parity)
  - F. Reset Counters to Zero
9. Console CY. CL. Picks
10. Forestroke
  - A. C. B. 8 Makes
  - B. MP 1 & All Buffers Reset = Prefix Record 2 Resets
  - C. Red Ribbon MAG. Drops
  - D. MP 3 = Write a 1 Bit
  - E. MP 5 = Write a 3 Bit
  - F. MP 9 = Write a 6 Bit
  - G. C. B. 8 Breaks
  - H. Pick Console CY. CL.
11. Backstroke
  - A. MP 1 = Backstroke Sets
  - B. Pick Forestep MAG.
  - C. MP 11 = Counter steps to one (Counter 1 thru 8)

NOTE: Items 10 & 11 will be repeated until the Counter Steps to 15 which will occur when MP 11 is coupled on the backstroke of the 15th cycle.

12. Forestroke of 16th Cycle
  - A. C. B. 8 Makes
  - B. MP 1 = Load 1 or Counter 16—45 Sets
  - C. MP 7 = Write a Search Bit
  - D. C. B. 8 Breaks
  - E. Pick Console CY. CL.

13. Backstroke of 16th Cycle
  - A. MP 1 = Backstroke Sets
  - B. Pick Forestep MAG.
  - C. MP 11 = Counters step to Zero (Counters 1 thru 8)

NOTE: Items 12 & 13 will continue until the Counter Steps to 14 which will occur when MP 11 is coupled on the backstroke of the 30th cycle.

14. Forestroke of 31st Cycle
  - A. C. B. 8 Makes
  - B. MP 1 = Load 2 or Counter 31—60 Sets
  - C. MP 10 = Write a 7 Bit
  - D. C. B. 8 Breaks
  - E. Pick Console CY. CL.
15. Backstroke of 31st Cycle
  - A. MP 1 = Backstroke Sets
  - B. Pick Forestep MAG.
  - C. MP 11 = Counters Step to 15 (On the next cycle they step to Zero)

NOTE: Items 14 & 15 will continue until the Counter Steps to 13 which will occur when MP 11 is coupled on the backstroke of the 45th cycle.

16. Forestroke of 46th Cycle
  - A. C. B. 8 Makes
  - B. MP 1 = Load 1 or Counter 16—45 Resets
  - C. MP 10 = Continue to write a 7 Bit
  - D. C. B. 8 Breaks
  - E. Pick Console CY. CL.
17. Backstroke of 46th Cycle
  - A. MP 1 = Backstroke Sets
  - B. Pick Forestep MAG.
  - C. MP 11 = Counter Steps to 14

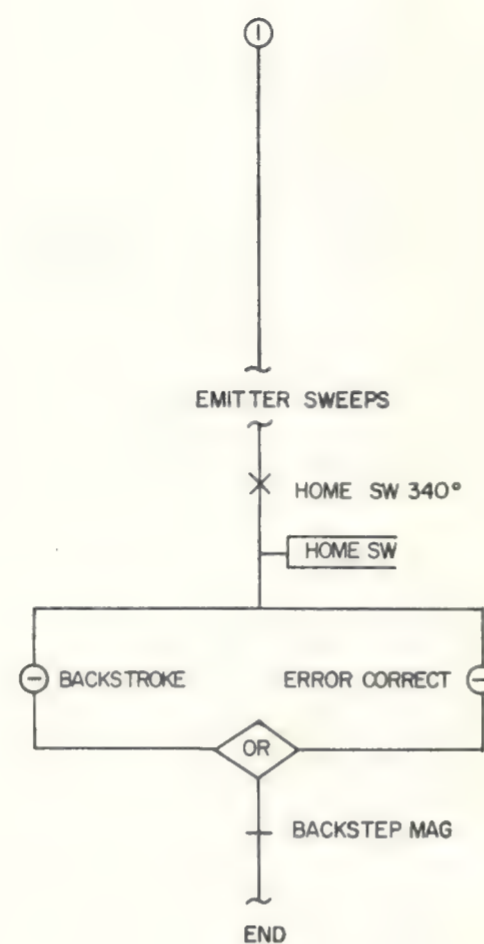
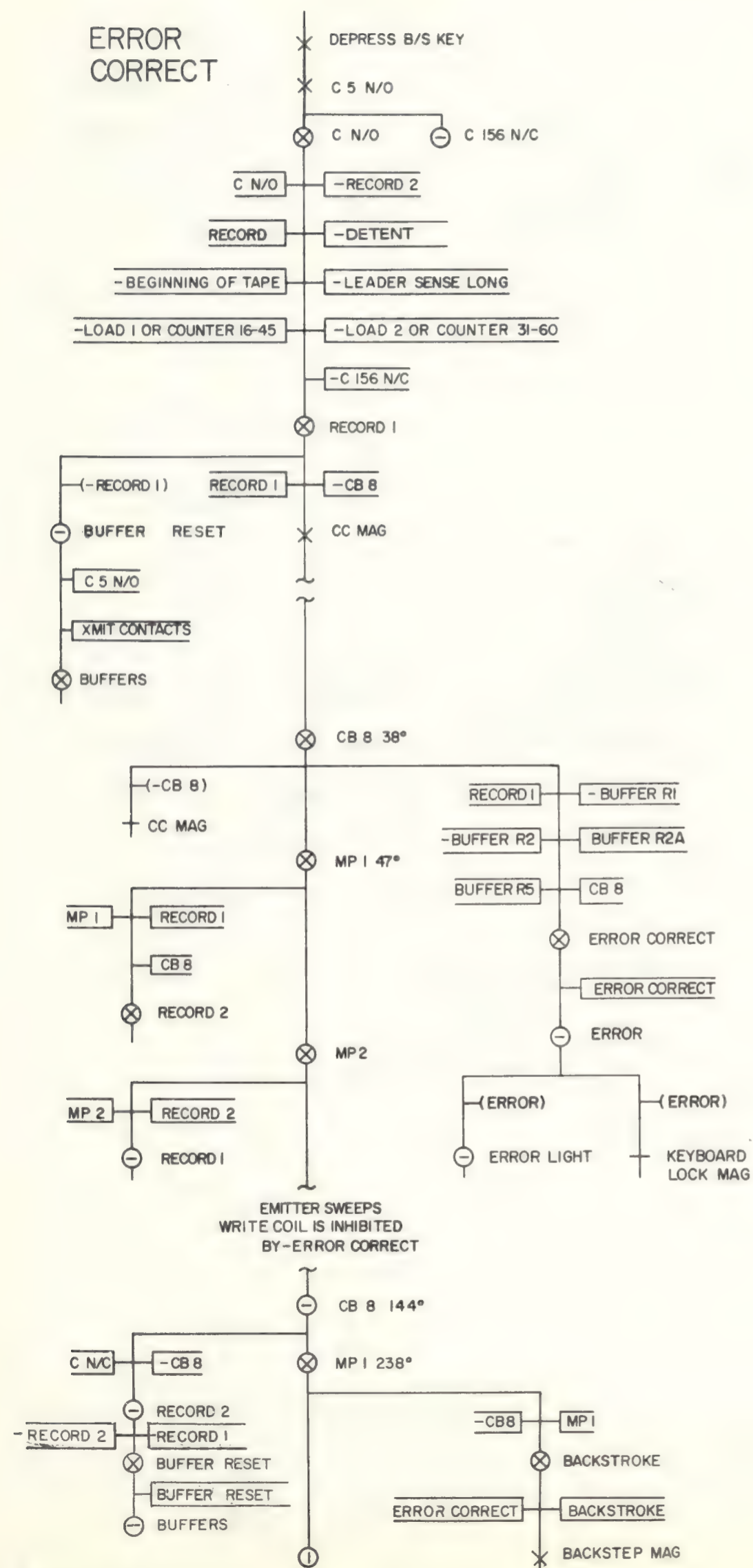
NOTE: Items 16 & 17 will continue until the Counter Steps to 12 which will occur when MP 11 is coupled on the backstroke of the 60th cycle.

18. Forestroke of 61st Cycle
  - A. C. B. 8 Makes
  - B. MP 1 = Reference Resets
  - C. MP 2 = Load 2 or Counter 31—60 Resets
  - D. MP 5 = Write a 3 Bit
  - E. C. B. 8 Breaks
  - F. Don't pick Console CY. CL. because Reference is reset
19. Backstroke of 61st Cycle
  - A. MP 1 = Backstroke Sets & Counters Reset
  - B. Pick Forestep MAG.
  - C. Bits read on Backstroke Steps Counter One
  - D. Parity check & Step Tape

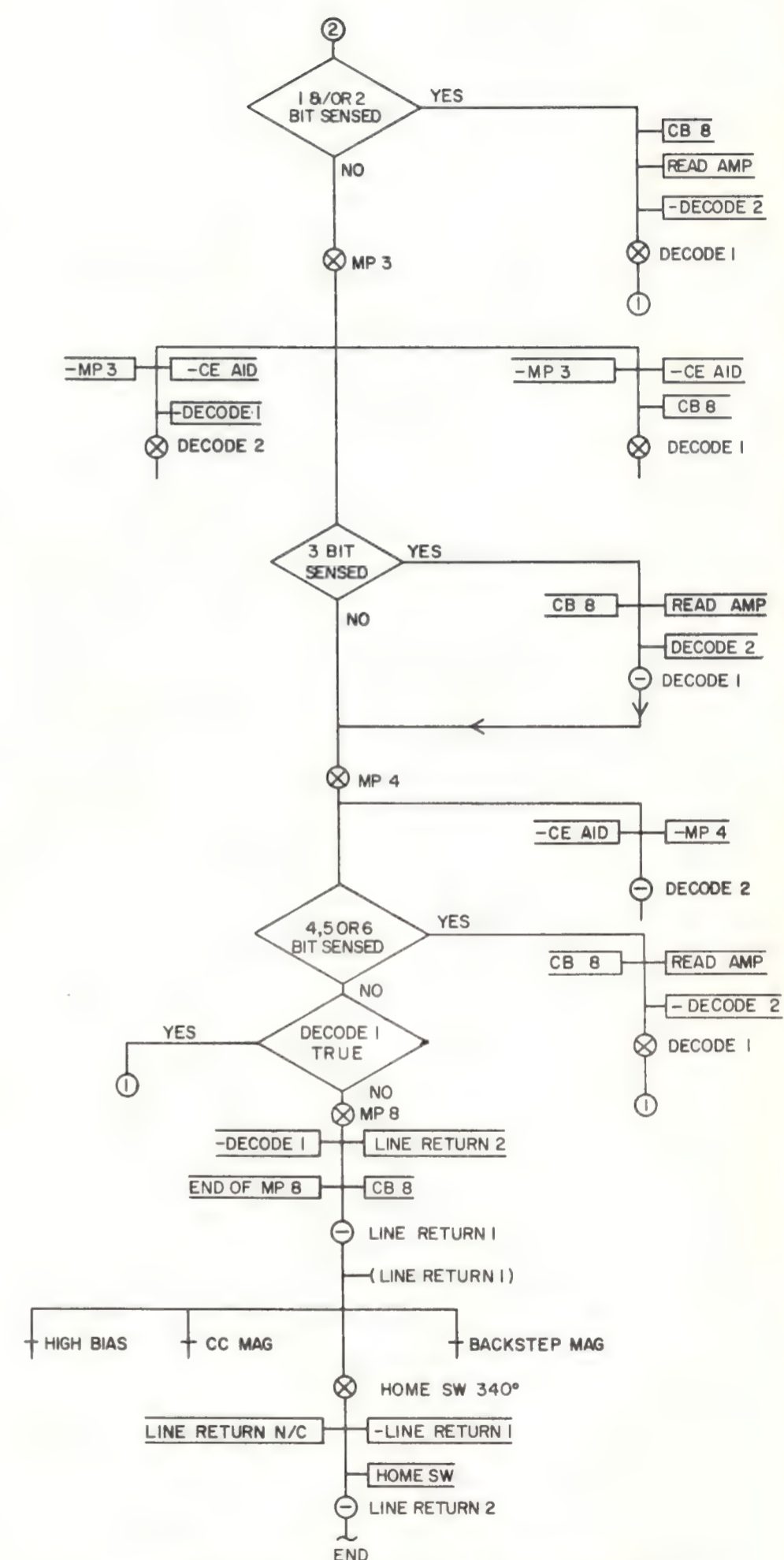
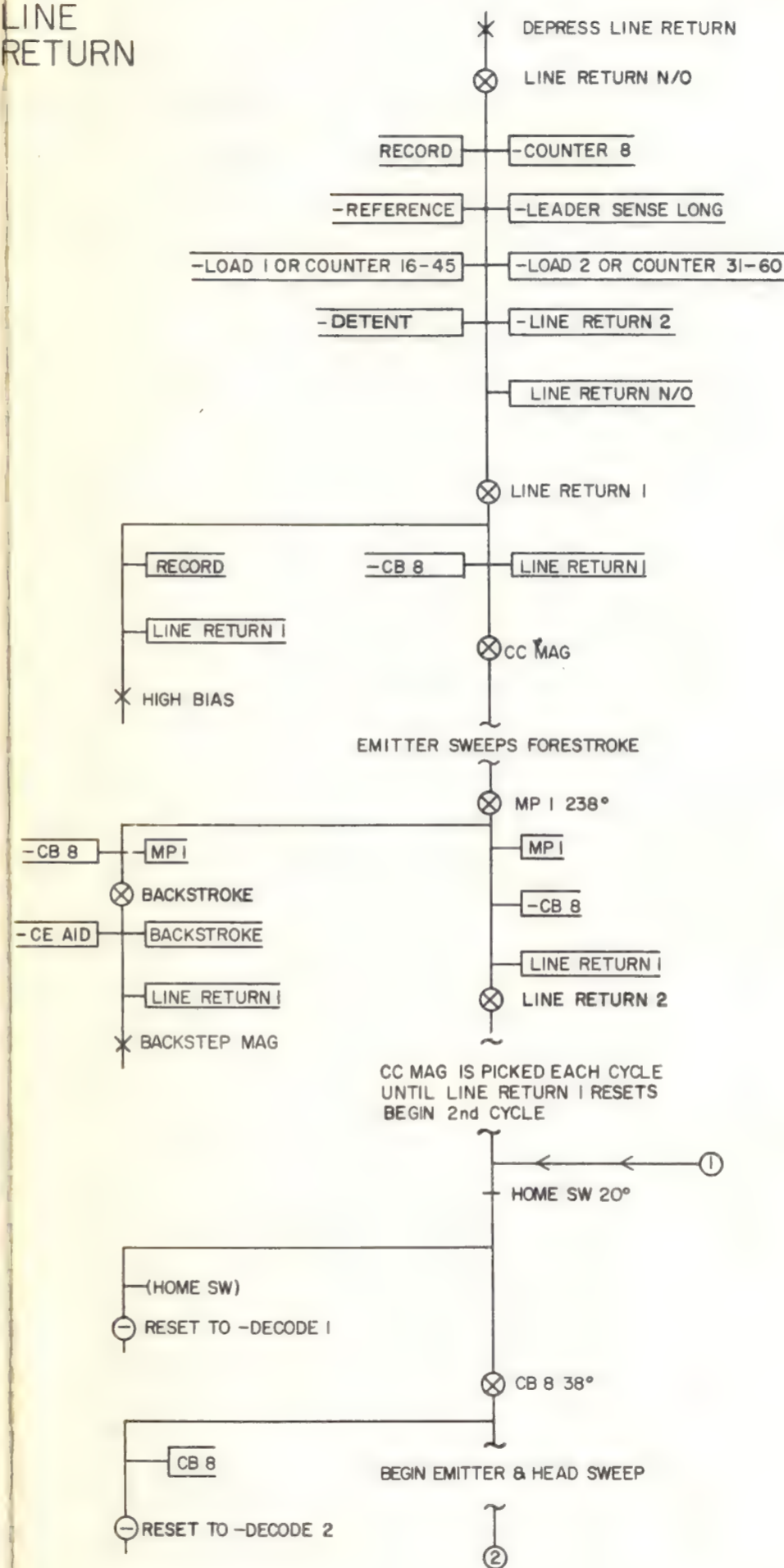




# ERROR CORRECT



# LINE RETURN

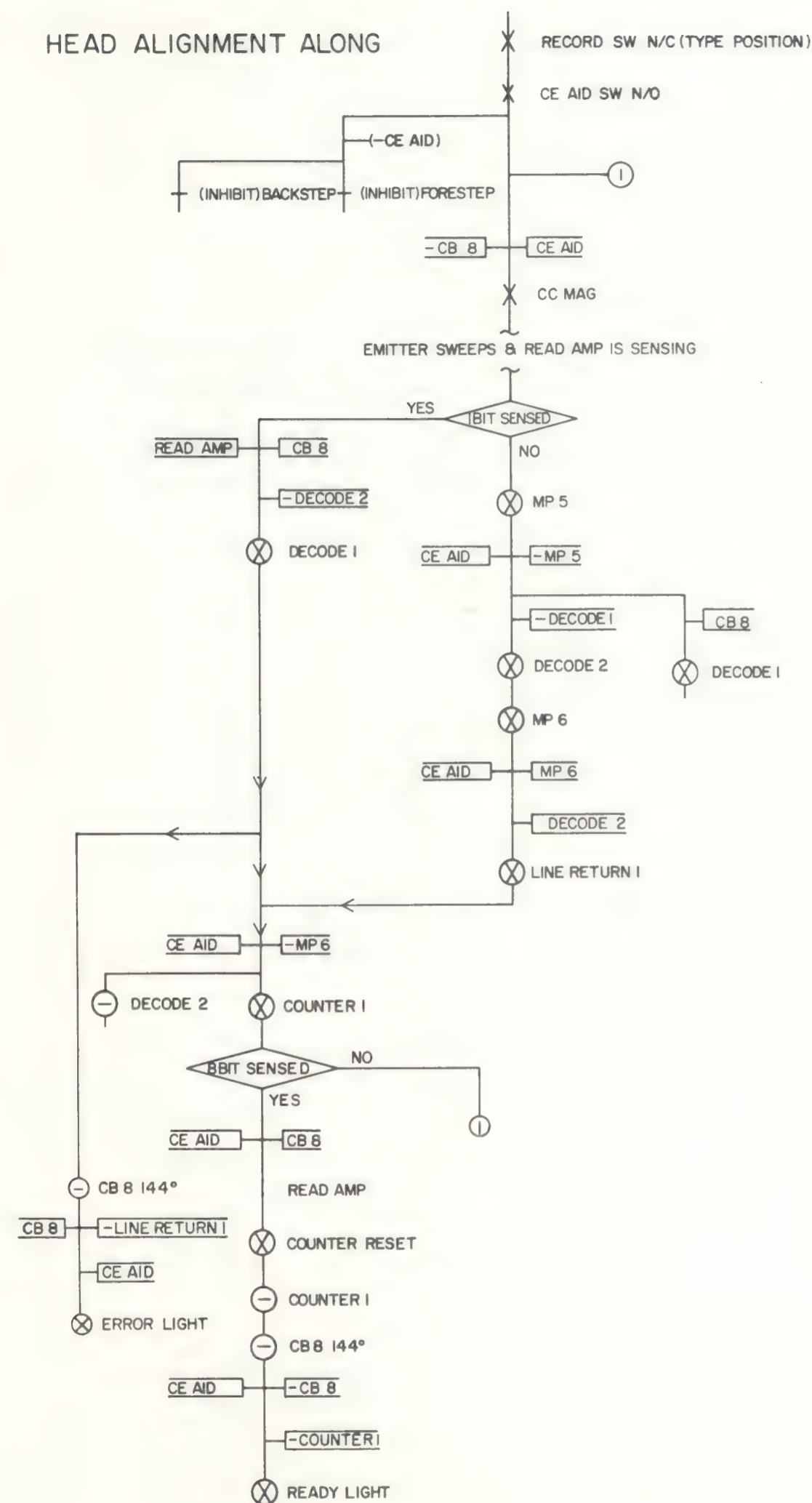


ERROR CORRECT, LINE RETURN

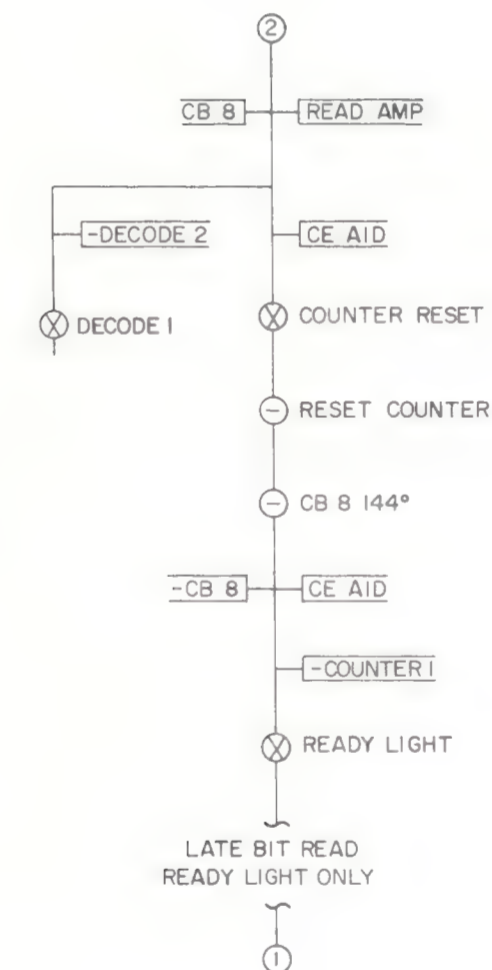
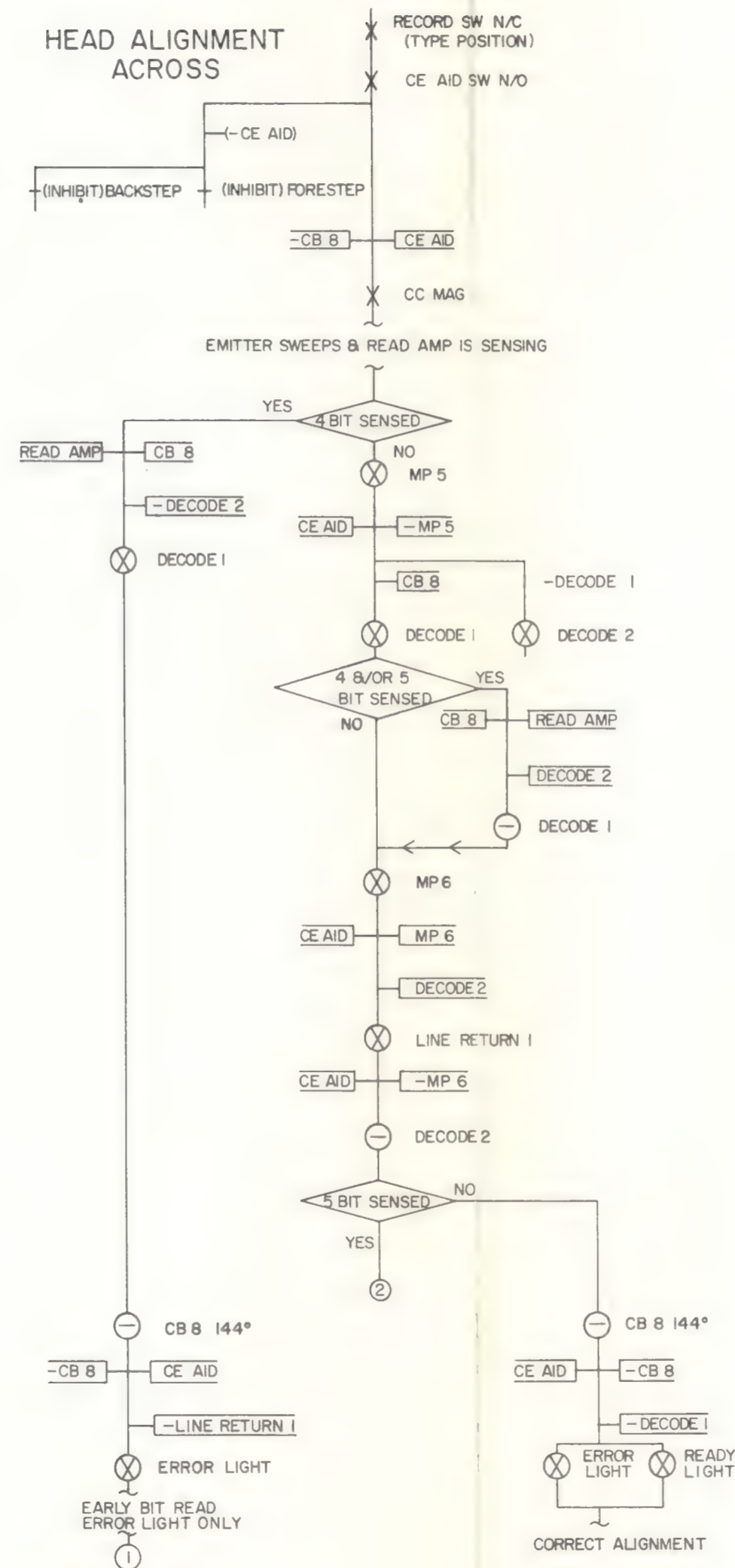
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# HEAD ALIGNMENT ALONG



# HEAD ALIGNMENT ACROSS

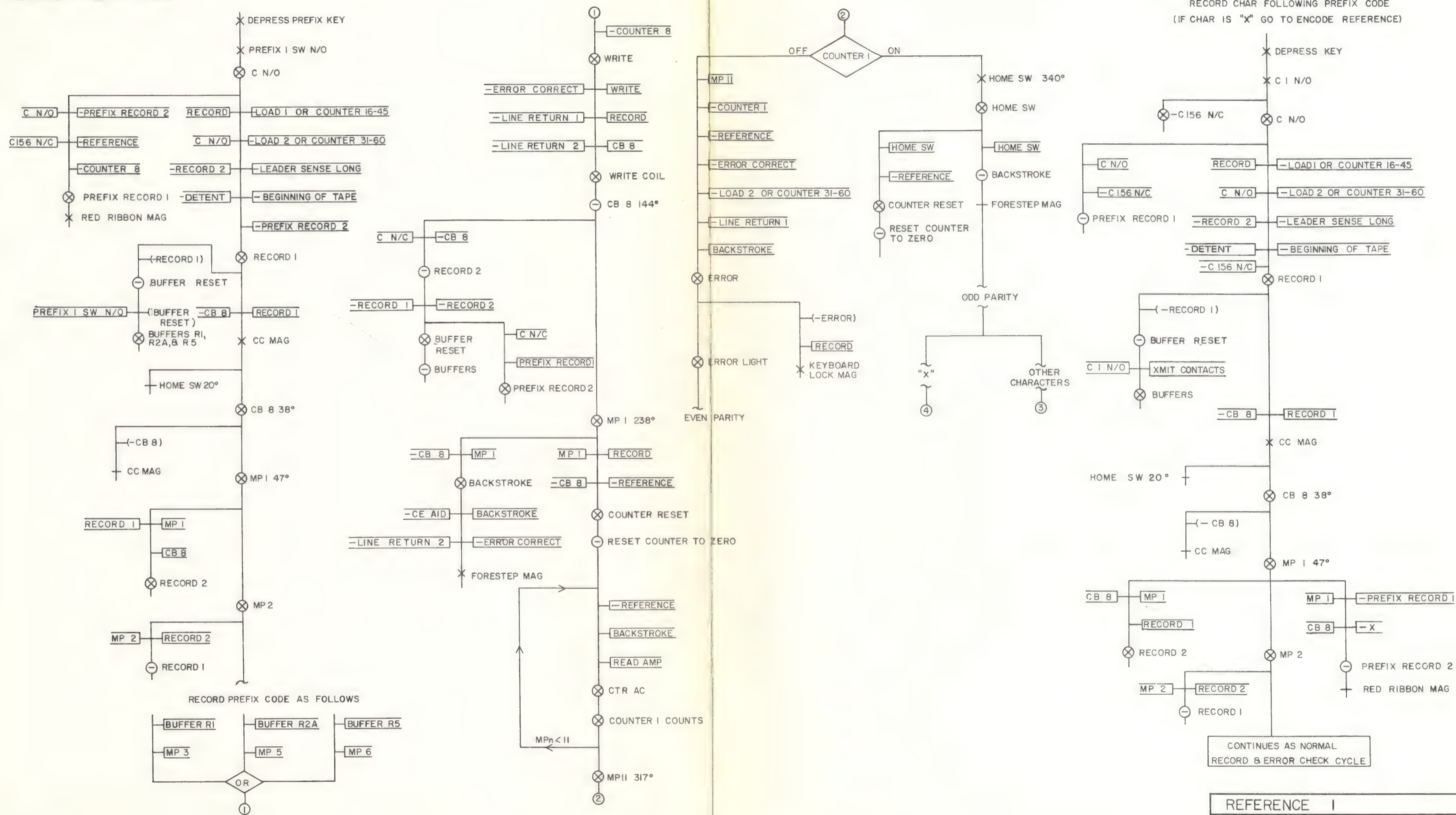


ALIGNMENT

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## RECORD PREFIX CODE



REFERENCE	I
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NOTE  
PREFIX RECORD 1 &  
PREFIX RECORD 2  
ARE UP & LATCHED

4

X DEPRESS "X" KEY

X C I N/O

X C N/O

X -C 156 N/C

C N/O

-C 156 N/C

PREFIX RECORD 1

RECORD

-LOAD 1 OR COUNTER 16-45

C N/O

-LOAD 2 OR COUNTER 31-60

-RECORD 2

-LEADER SENSE LONG

-DETENT

-BEGINNING OF TAPE

-C 156 N/C

X RECORD

(-RECORD 1)

BUFFER RESET

C I N/O

XMT CONTACTS

X BUFFERS

-CB 8

RECORD 1

X CC MAG

HOME SW 20°

X CB 8 38°

(-CB 8)

CC MAG

X MP 1 47°

MP 1

RECORD 1

CB 8

X RECORD 2

MP 2

RECORD 2

MP 2

RECORD 1

RECORD "X" AS FOLLOWS

BUFFER R5

MP 6

-COUNTER 8

BUFFER T1

MP 8

BUFFER CK

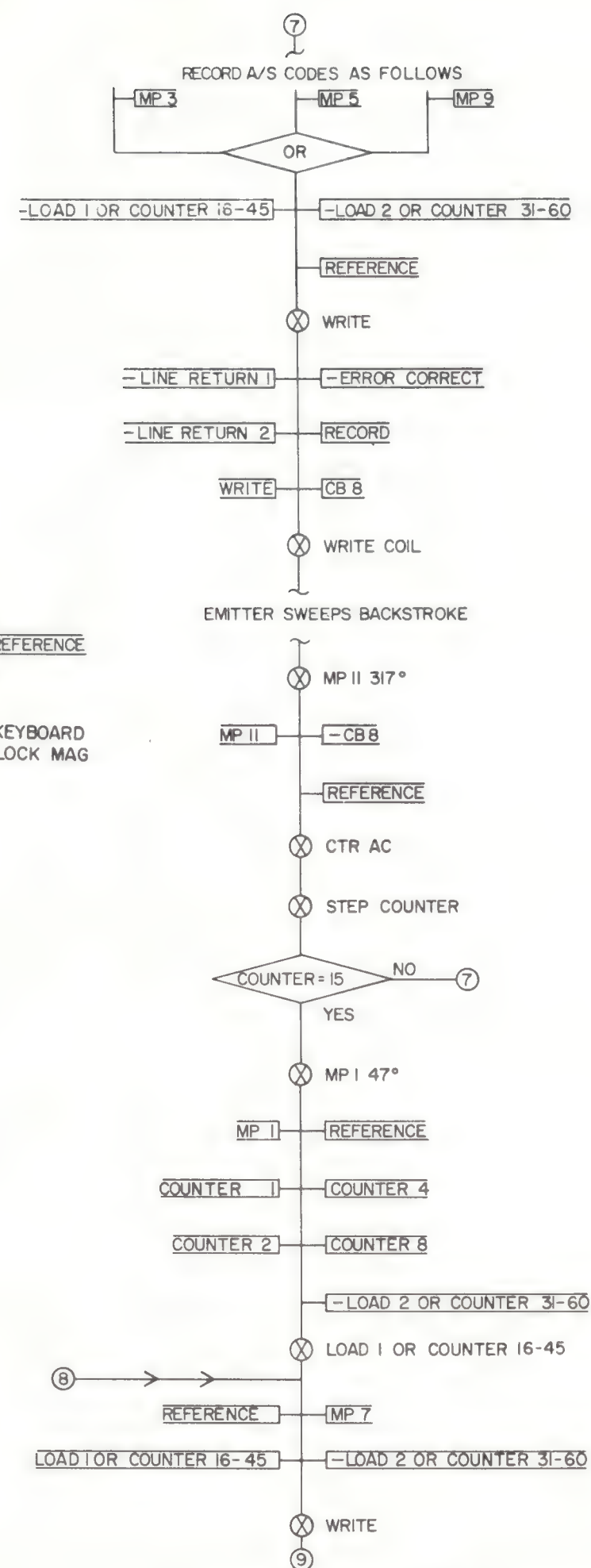
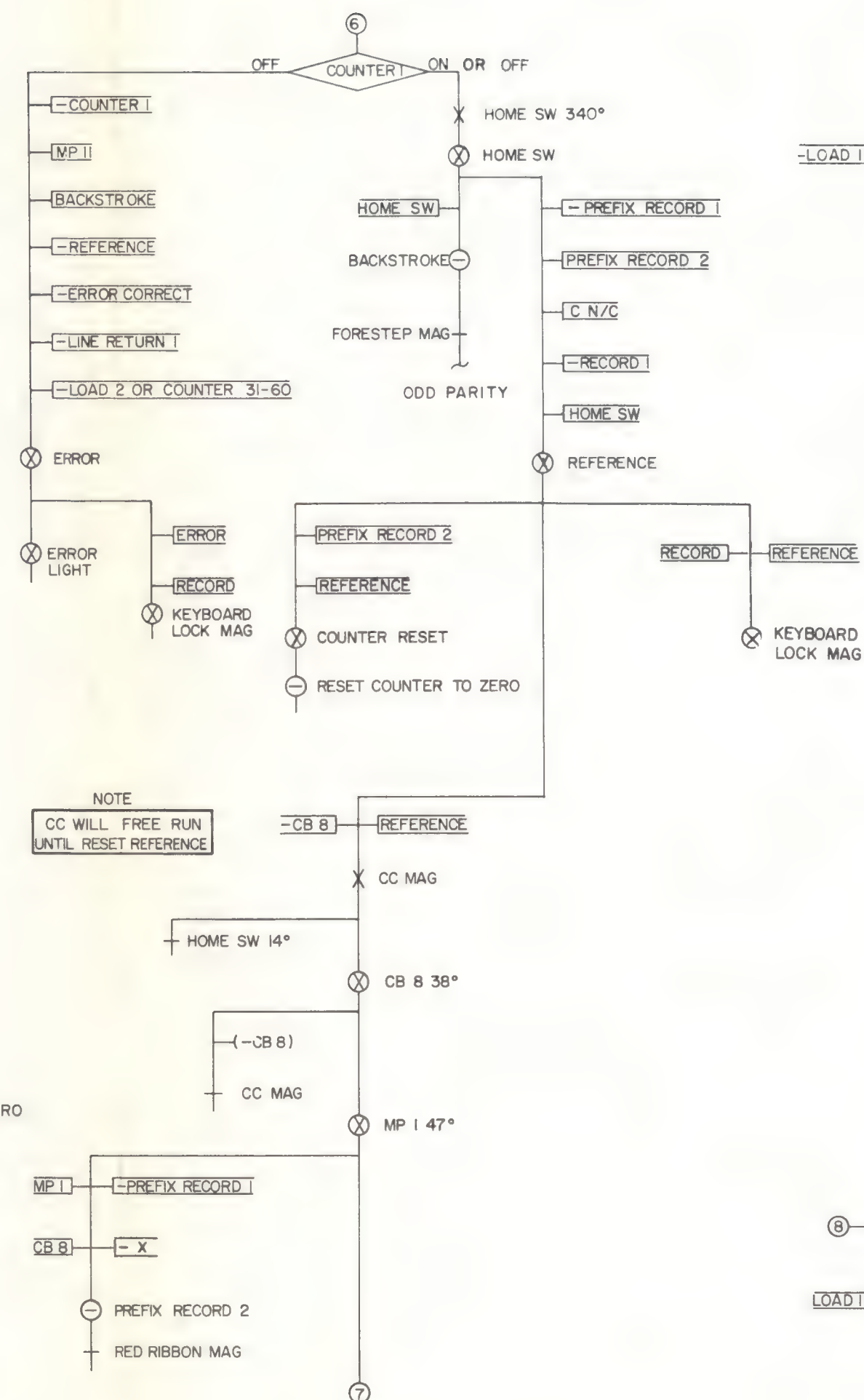
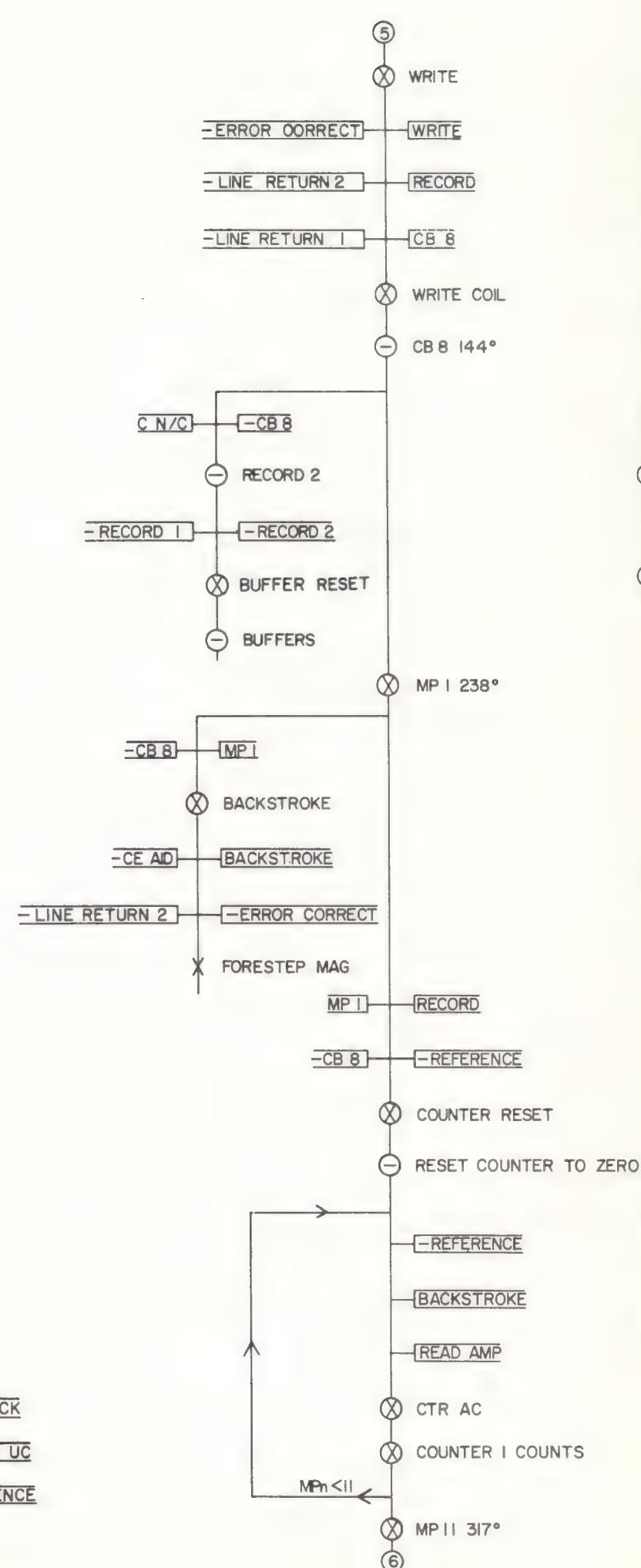
-BUFFER UC

MP 10

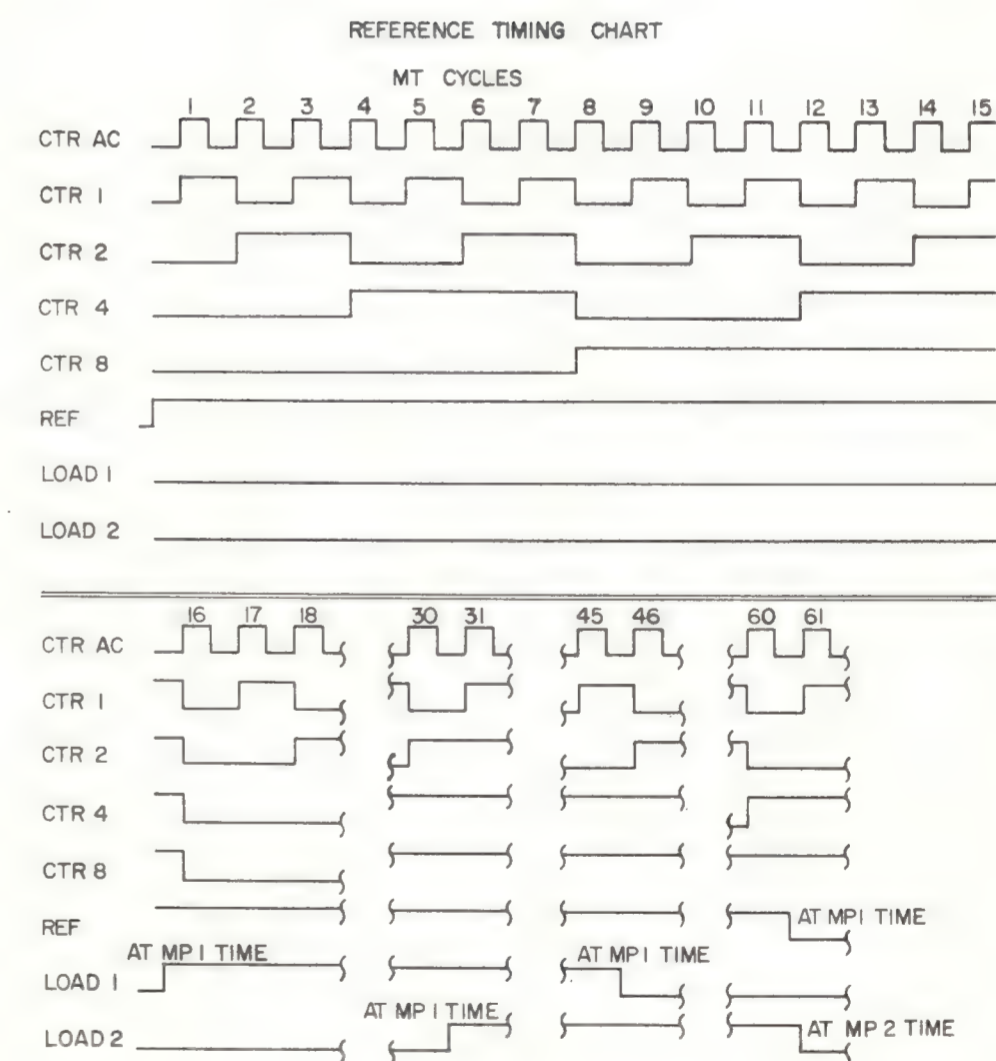
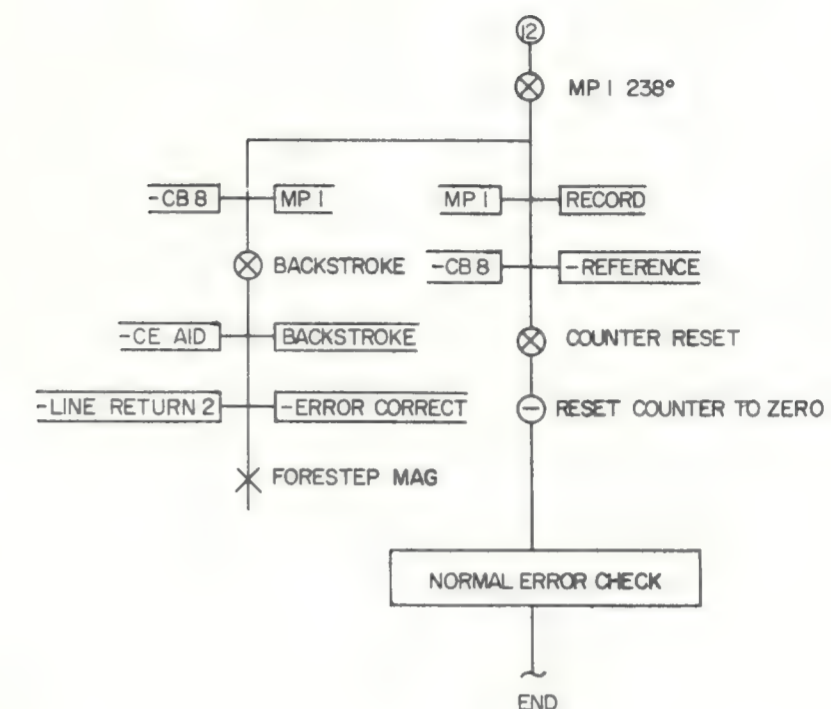
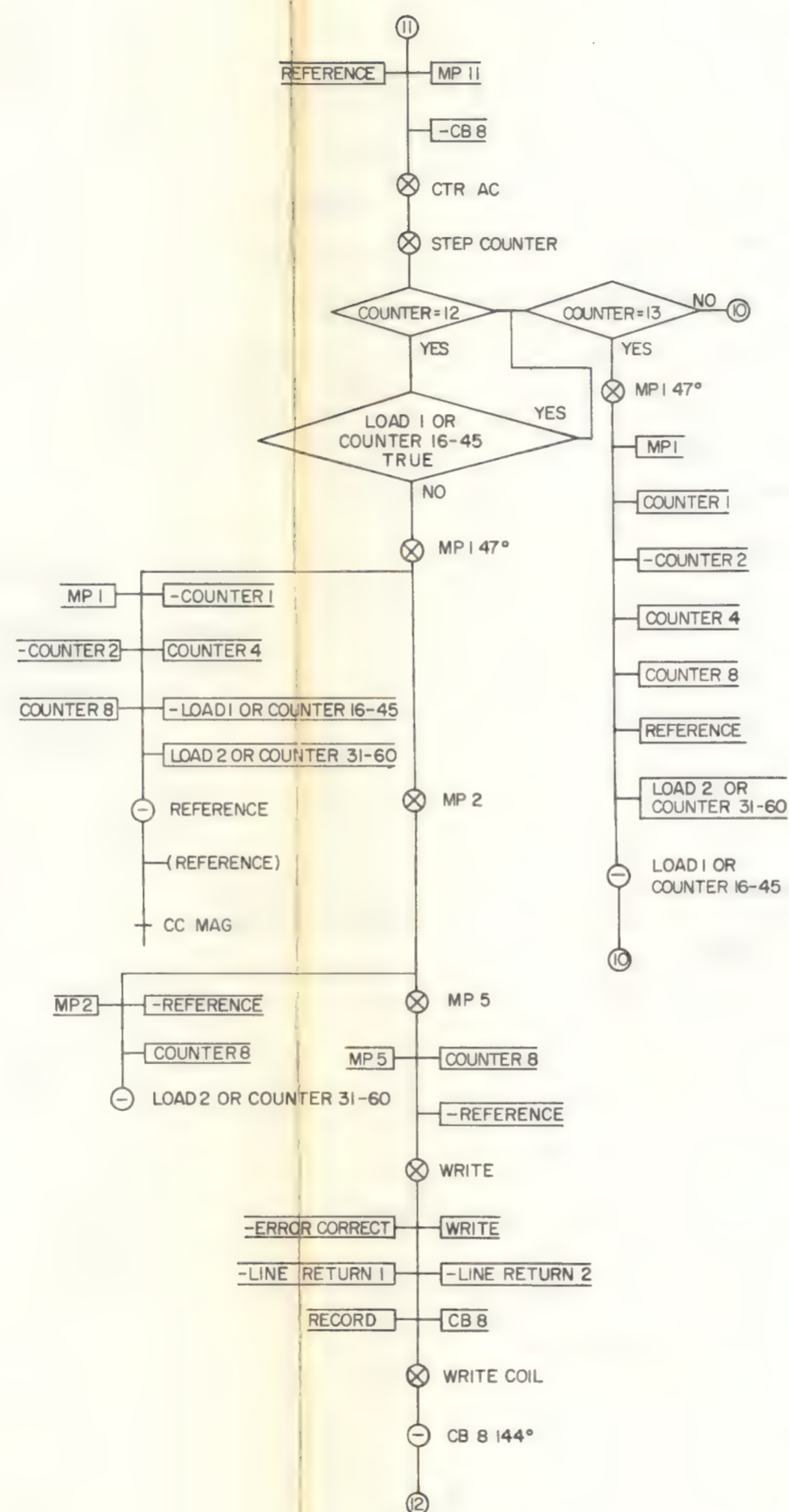
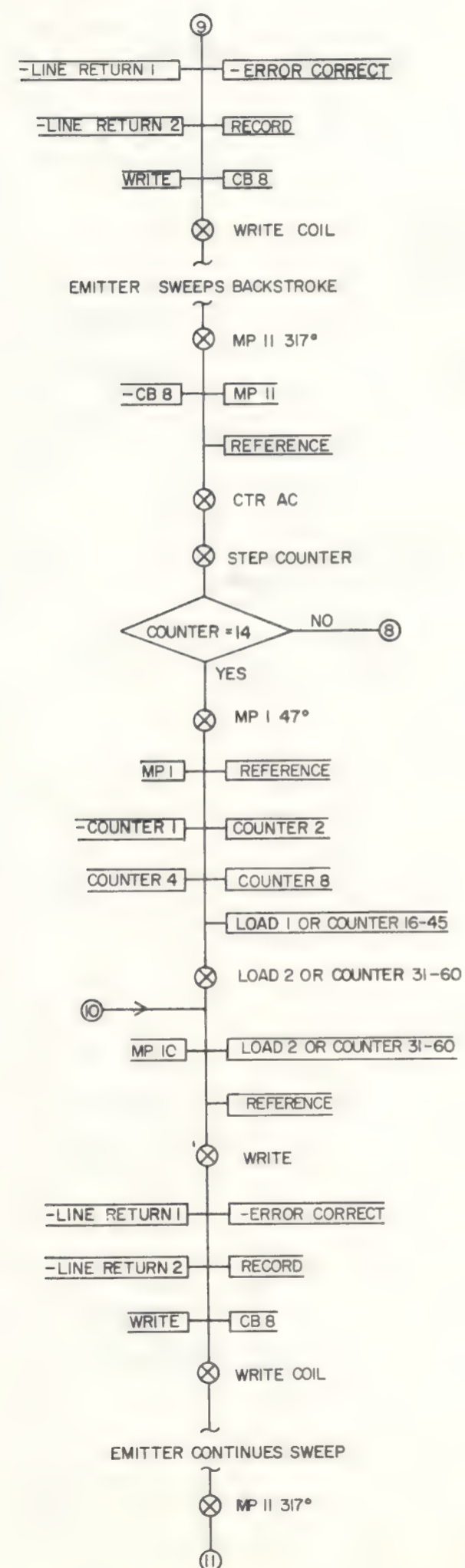
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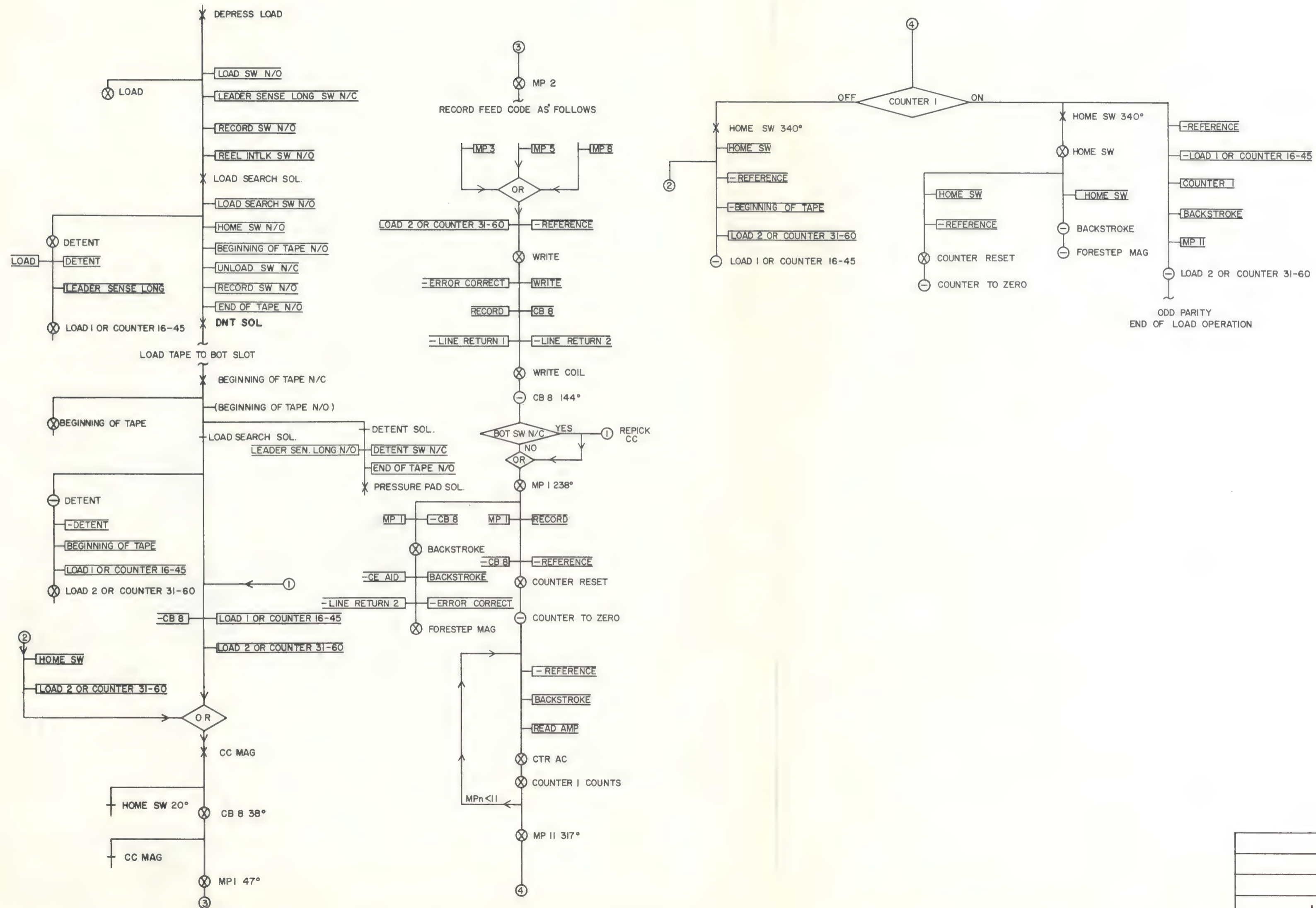
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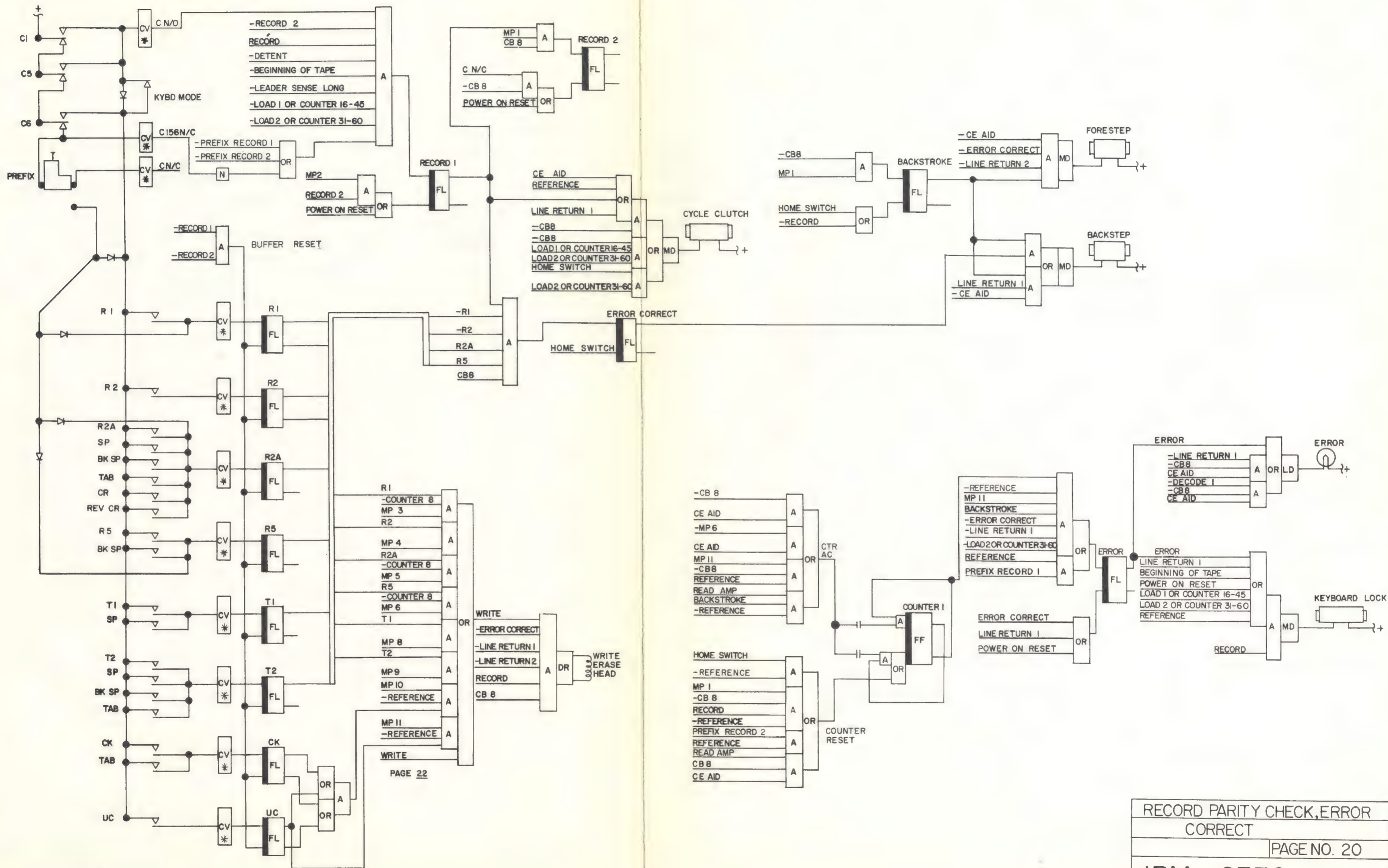


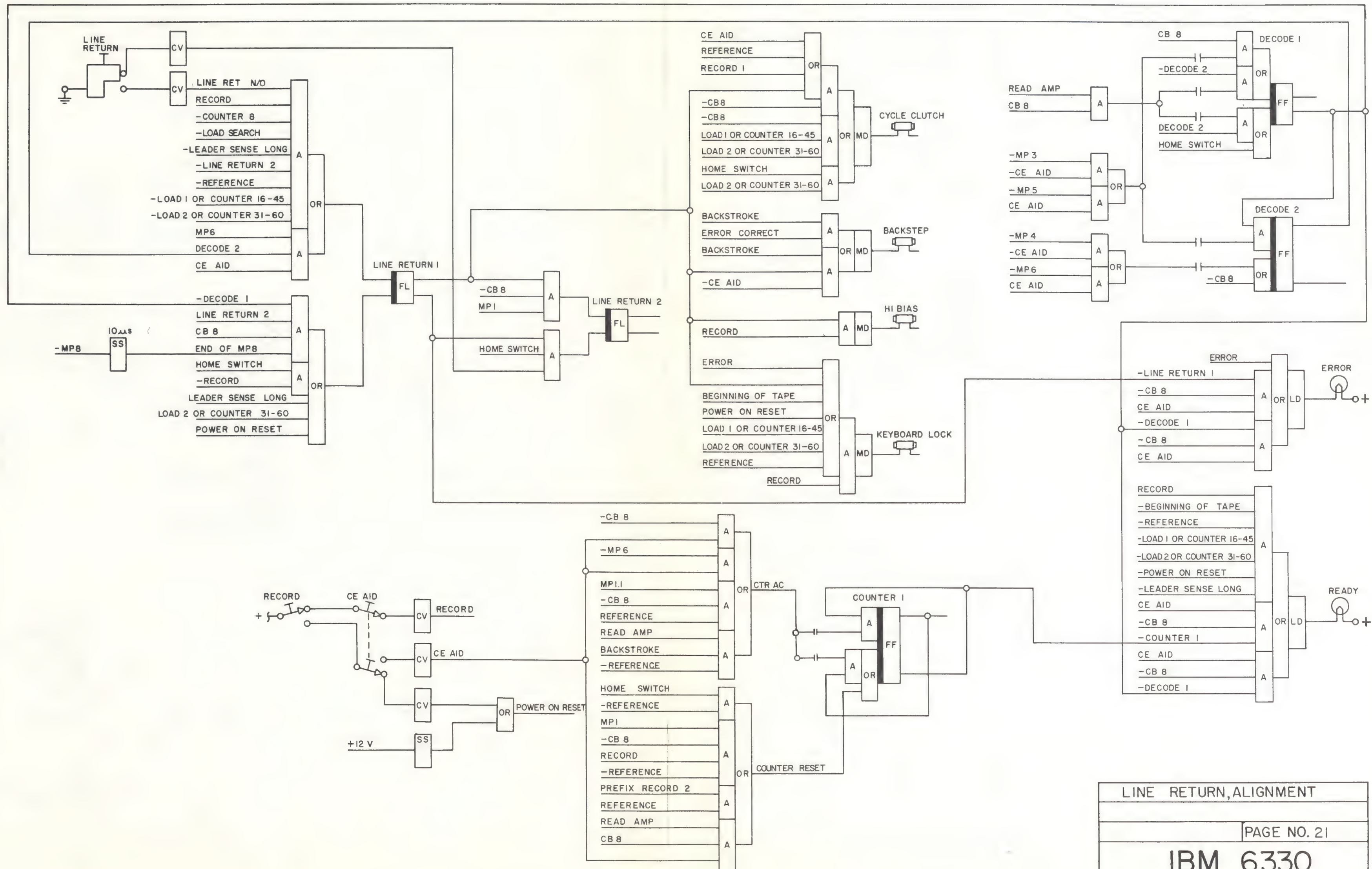
# IBM 6330

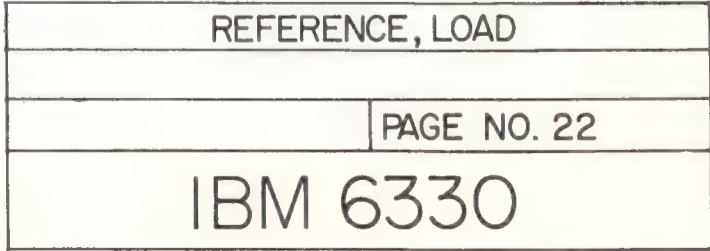


# LOAD











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ILD, Sequence Charts, Function Charts

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## IMPROVED SEARCH FEATURE MT/SC

An improved Search Feature has been incorporated into four new Precons recently released as an SER for the MT/SC.

Four terms used relative to this feature are defined as follows:

1. Panel Search — A Search operation initiated at the CCU Control Panel.
2. Tape Search — A Search operation initiated by a code read from the tape.
3. Incremental Search — Moving the tape forward or backward a given number of increments (Reference codes) from the point the tape was resting when the Search was initiated.
4. Absolute Search — Searching the tape to a specific Reference code, counting from the beginning of the tape. An Absolute Search always involves rewinding the tape before searching back out to the Absolute Reference code.

With this feature, the tape may now be searched in one of three ways, according to the Precon being used:

1. The Search keybutton on the reader still searches the tape or tapes (if both are loaded) ahead one increment for each depression of the button.
2. With the proper Precon loaded (presently this includes 340, 341, 342 & 343) a Control Panel entry can be made as follows:
  - a. Search the right tape to any Reference code from 1 to 127, or
  - b. Search the left tape to any Reference code from 1 to 127, or
  - c. Search both tapes to any Reference code from 1 to 127.

*NOTE: Items 2a, b & c are Absolute Search operations.*

3. In addition to the "Panel Search" explained in item 2, some Precons (presently 340 & 342) will allow "Tape Search" or Search operations initiated by codes read from the tape. This type of search is more flexible in that the system, on tape command can:
  - a. Do an Absolute Search of the opposite tape (from which the code was read) or the same tape (not both) to any Reference code, 1 thru 127.
  - b. Do an Incremental Search of the opposite tape or the same tape (not both), either forward or backward, any given number of Reference codes from 1 thru 63.

The procedure to follow in initiating a Tape Search or a Panel Search will depend on the Precon used. The information on each Precon will contain these instructions.

These improved abilities of searching the tape are a function of the program, therefore a Precon having this capability must be used.

In addition to the proper Precon, the MT/SC is also modified as follows:

1. A board change is required.
2. Three SLT/SLD cards are added.
3. Some wiring changes on the SMS Block in the reader are required.
4. One SMS card added to the reader.

### PROGRAM SEARCH

Panel Search and Tape Search are grouped together and considered Program Search operations. This is because they are functions of the Precon.

Reading Tape Search instructions from the tape or keying these instructions in at the Control Panel when the Panel Search Light is on, will cause the Precon to respond with one of the following:

1. An Output to device code 6 Program Step if the right station is to be searched.  
*Example: ot6, 4*

op1	op2	op3	op4	op5	8	4	2	1	op6	op7
0	0	0	1	0	0	1	1	0	0	0

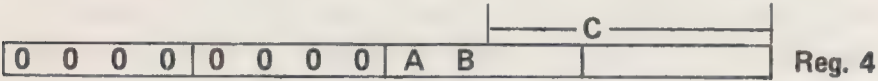
2. An Output to device code 2 Program Step if the left station is to be searched.  
*Example: ot2, 4*

op1	op2	op3	op4	op5	8	4	2	1	op6	op7
0	0	0	1	0	0	0	1	0	0	0

This Program Step will call for an Output to the particular device code from a specific Register such as Register 4. This Register will have been conditioned by the Precon in accordance with the search instructions.

The following information is for an Incremental Search. Remember, Incremental Search is initiated by instructions read from the tape. The maximum increment is 63.

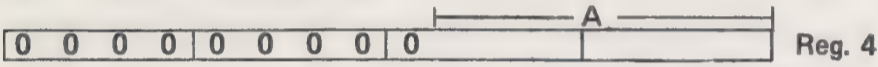
This is the register to Output from, not the Program Step:



- A. This eight bit being ON denoted Incremental Search, OFF denotes Absolute Search.
- B. This 7th bit ON in conjunction with the 8th bit ON denotes Forward Search, OFF with the 8th bit ON denotes Reverse Search.
- C. The 1st thru the 6th bits are used to indicate the binary value of the Increment desired. All 6 ON = 63.

The following information is for an Absolute Search. Remember, Absolute Search can be initiated by instructions read from the tape or entered at the Control Panel. (When entering at the Control Panel, the Panel Search light must be on.)

This is the Register to Output from, not the Program Step:



- A. The 1st thru the 7th bits are used to indicate the binary value of the increment desired. All 7 ON = 127.

*NOTE: As a Service Aid, an Incremental Search can be keyed in at the Control Panel.*

With the Panel Search light ON, the following will work as indicated:

1. Reverse Search 1 Increment — Key 1, 2, 9, Station desired (or both) and Start. For 2 Increments, Key 1, 3, 0; for 3 Increments, Key 1, 3, 1; etc.
2. Forward Search 1 Increment — Key 1, 9, 3, Station desired (or both) and Start. For Forward 2 Increments, Key 1, 9, 4; for 3 Increments, Key 1, 9, 5; etc.

The following pages contain Sequence Charts; Function Charts & Intermediate Logic Diagrams (ILD's).

The Sequence Charts and/or the Function Charts can be used to follow each operation through the ILD's. The sequence charts do not necessarily list all the inputs required to "bring up" the next signal, but enough are listed to ensure that the proper logic block is used.

## MANUAL SEARCH

The Manual Search Keybutton on the Reader will be operative if the Right Tape is loaded. If both tapes are loaded, depressing the Keybutton will cause both to be searched forward one Reference code.

### RIGHT STATION

#### A. DEPRESS THE SEARCH KEYBUTTON

1. Sch Keybutton = Sch Key $\uparrow$  = Sch Key TM $\uparrow$  & Manual Sch sets
2. Sch Key TM = Set 14 $\uparrow$  = 14 Count $\uparrow$  = Err Lite $\uparrow$  & Sta RT sets = Sta LF $\downarrow$  = PP LF down = PP RT picks
3. Manual Sch & 14 Ct = Trf Sch Sta sets if If tape is loaded
4. 14 Ct = Sch $\uparrow$  = Sch Pos Mag Log can't come up
5. Sch & Home = pick Cy Cl

#### B. LATCH HEAD OUT

1. Sch Pos Cont = Sch Pos $\uparrow$
2. Let Sch Keybutton up = Sch Key $\downarrow$
3. -Sch Key & Sch Pos = Sch Pos TM $\uparrow$
4. Sch Pos TM & Manual Sch = Stop Sch $\uparrow$  & Ld Sch Sol Log TM $\uparrow$
5. Ld Sch Sol Log TM = Ld Sch Shaft moves = Ld Sch Sol Sw $\uparrow$
6. Sch Pos TM & 14 Ct & Ld Sch Sol Sw = Dnt RT Sol Log $\uparrow$
7. Dnt Rt Sol Log = Dnt RT picks = Sch shoe on spring clutch

#### C. TAPE MOVEMENT WITH PRESSURE PAD UP

1. A single bit in ctr channel = Sch Bit $\uparrow$  = MT Bit $\uparrow$
2. MT Bit & Stop Sch = MT RD Lat Set $\uparrow$
3. MT RD Lat Set & Sch Bit = MT RD sets = -MT RD $\downarrow\downarrow$
4. -MT RD down = drop Dnt & Ld Sch shaft & Sch Pos mag picks

#### D. TAPE STOPS AND HEAD SLIDE GOES HOME

1. Sch Pos down = Sch Pos TM $\downarrow$  = Stop Sch $\downarrow$  = MT RD Lat Set $\downarrow$
2. MT RD & -Dnt Out & Home = Set 0 $\uparrow$  = Reset Data Lats & 14 Ct $\downarrow$  = Sch $\downarrow$
3. MT RD = Man Sch $\downarrow$  if Trf Sch Sta is down
4. -Sch Pos TM & -10 Ct & Sta Rt = pick Cy Cl

#### E. FIRST CYCLE

1. MT RD & 10 Ct = Incr sets = step tape each cycle (Home = Incr resets)
2. MT RD & 10 Ct = pick Cy Cl

#### F. 2nd AND SUCCESSIVE CYCLES

1. MT RD & Home = Set 0 $\uparrow$  = reset Data Lats each cycle

#### G. 3 BIT SENSED

1. DL 3 & -DL 6 & 10 CT (ILD P. 0301) = Car Rtn $\uparrow$  = MT RD resets
2. MT RD down = don't repick Cy Cl or reset Data Lats
3. MT RD down also = Err Lit out unless Trf Sch Sta is up

Manual Search Right ends with 10 Ct & DL 3 set.

### LEFT STATION

If the Left Station is loaded when the Right Station is Manually Searched, the Transfer Search Station latch will set. This will cause the Left Station to be searched.

#### A. IF TRANSFER SCH STATION IS SET

1. Trf Sch Sta & 10 Ct & Home & -MT RD = Sta Rt resets
2. Sta Rt down = Sta Lf $\uparrow$  = Lf PP Sol Log $\uparrow$  = PP Rt $\downarrow$
3. Trf Sch Sta & Sta Lf = Sch $\uparrow$  = Reset DL 3 $\uparrow$  (ILD P. 0302)
4. Sch & -MT RD = Sch Pos Mag Log can't come up
5. Sch & Home = Pick Cy Cl

#### B. LATCH HEAD OUT

1. Sch pos Cont = Sch Pos $\uparrow$
2. Sch Pos & -Sch Key = Sch Pos TM $\uparrow$
3. Sch Pos TM & Manual Sch = Stop Sch $\uparrow$  & Ld Sch Sol Log TM $\uparrow$

4. Ld Sch Sol Log TM = Ld Sch Shaft moves = Ld Sch Sol SW $\uparrow$
5. Ld Sch Sol Sw & Sta Lf & Trf Sch Sta & Sch Pos TM = Dnt Lf Sol Log $\uparrow$
6. Dnt Lf Sol Log = Dnt Lf picks & sch shoe on spring clutch

#### C. TAPE MOVEMENT WITH PRESSURE PAD UP

1. A single bit in ctr channel = Sch Bit $\uparrow$  = MT Bit $\uparrow$
2. MT Bit & Stop Sch = MT RD Lat Set $\uparrow$
3. MT RD Lat Set & Sch Bit = MT RD sets = -MT RD $\downarrow\downarrow$
4. -MT RD down = drop detent & Ld sch shaft & pick sch pos mag

#### D. TAPE STOPS AND HEAD SLIDE GOES HOME

1. Sch Pos down = Sch pos TM $\downarrow$  = Stop Sch $\downarrow$  = MT RD Lat Set $\downarrow$
2. MT RD & Sta Lf = Trf Sch Sta resets = Sch $\downarrow$  & Manual Sch resets
3. MT RD & -Dnt Out & Home = Set 0 $\uparrow$  = reset Data Lats
4. -Sch Pos TM & -10 Ct & Sta Lf = pick Cy Cl

#### E. FIRST CYCLE

1. MT RD & 10 Ct = Incr sets = step tape each cycle (Home = Incr resets)
2. MT RD & 10 Ct also = pick Cy Cl

#### F. 2nd AND SUCCESSIVE CYCLES

1. MT RD & Home = Set 0 $\uparrow$  = reset Data Lats each cycle

#### G. 3 BIT SENSED

1. DL 3 & -DL 6 & 10 Ct (ILD P. 0301) = Car Rtn $\uparrow$  = MT RD resets
2. MT RD down = don't repick Cy Cl or reset Data Lats
3. MT RD down also = Err Lit out

## ABSOLUTE SEARCH

An Absolute Search can be initiated by a Tape Search code or from the Control Panel. In either case, the Search Operation is caused by an Output to the Reader P.S. If "BOTH" is answered at the Control Panel, two P.S.'s will be performed and the Right Station will always be searched first.

Absolute Search always involves rewinding the tape. Because of the Unload Was Last Function flip latch, a Program Search cannot follow unloading one of the Tapes.

### ABSOLUTE SEARCH RIGHT STATION

#### A. OUTPUT TO DEVICE 6 P.S.

1. I-2 of Output P.S. = Dev Cde 6↑ & Sel Opt Dev↑ = Sch Rt sets = Prog Sch Op↑
2. I-5, B1-4 & B5-8 = Reset & Load Output Latches to value desired
3. Output 8 being down = Incr Sch stays down = Absolute Sch stays up
4. I-5, B13-16 = Bsy sets = Rdy resets
5. Bsy & Prog Sch Op = Prog Sch↑ = Sch In Prog↑ = Err Lite TM↑ = Err lite on
6. Prog Sch & Sch Rt = -Sta Lf TM↑ = Sta Rt sets = Sta Lf↓
7. -Rewond & Prog Sch & Absol Sch = Rev Motn sets
8. Rev Motn & Absol Sch & -Sta Lf TM = Lf PP Sol Log↑↑
9. Lf PP Sol Log = Lf PP up if Lf tape is loaded = Rt PP down  
NOTE: Tape will rewind with Rt PP up if LF Sta is unloaded.
10. Rev Motn & Sch Rt = Dnt Rt & Hi Bias picks

#### B. TAPE REWINDS

1. Rewind Sense Sw = Rew Sen↑
2. Rew Sen & Absol Sch = Rewond sets
3. Rewond = Rev Motn resets & -MT RD = Sch↑
4. Rev Motn down also = drop Dnt Rt & Hi Bias Rt & Lf PP

#### C. TAPE STOPS

1. Lf PP down = Rt PP up
2. Sch & -MT RD = Sch Pos Mag can't pick
3. Sch & -MT RD & Home = pick Cy Cl

#### D. LATCH HEAD OUT

1. Sch Pos Cont = Sch Pos↑
2. Sch Pos & -Manual Sch = Sch Pos TM↑
3. Sch Pos TM & Rewond = Fwd Motn sets = Sch Key TM↑ = Set 14↑
4. Set 14 = 14 Ct↑
5. Sch Pos TM & Fwd Motn = Ld Sch Sol picks
6. 14 Ct & Sch Pos TM = Dnt Rt picks

#### E. TAPE MOVES WITH PRESSURE PAD UP

1. Bits sensed in ctr channel = Sch Bit↑ (300 u sec) = MT Bit↑ (10 u sec)
2. MT Bit & Sch Pos TM = MT Bit SS↑ (400 u sec)
3. approximately 7 MT Bit SS's = Ref Det↑
4. Ref Det & Prog Sch = Ref Ctr AC↑ = -Ref Ctr AC↓ = step ctrs
5. when ctrs = value in Output Lats = Eq Ct↑
6. Eq Ct & Ref Det = Stop Sch↑ = MT RD Lat Set↑ = MT RD sets
7. MT RD & Prog Sch Op = Sch IF TM↑ = OIF\* sets = Bsy resets = Prog Sch↓
8. -MT RD down = drop Dnt Rt & Ld Sch Sol & pick Sch Pos Mag

#### F. TAPE STOPS AND HEAD SLIDE GOES HOME

1. Sch Pos down = Sch Pos TM↓
2. MT RD = Fwd Motn resets = Sch Key TM↓ = Set 14↓
3. MT RD & -Dnt Out & Home = Set 0↑ = reset Data Lats & 14 Ct↓ = Sch↓  
NOTE: MT RD keeps Err lite on & Sch In Prog up.
4. -Sch Pos TM & -10 Ct & Sta Rt = pick Cy Cl

#### G. FIRST CYCLE

1. MT RD & 10 Ct = Incr sets = step tape each cycle (Home = Incr resets)
2. MT RD & 10 Ct = pick Cy Cl

#### H. 2nd AND SUCCESSIVE CYCLES

1. MT RD & Home = Set 0↑ = reset Data Lats each cycle

#### I. 3 BIT SENSED

1. DL 3 & -DL 6 & 10 Ct (ILD P. 0301) = Car Rtn↑ = MT RD resets
2. MT RD down = don't repick Cy Cl or reset Data Lats
3. MT RD down also = Err Lite↓ & Sch In Prog↓ & Sch IF TM↓
4. -Sch IF TM = OIF\* resets = Rdy can set

Absolute Search Right ends with Sch Rt, Prog Sch Op, Rewond & Eq Ct all up. They will go down with the next Deselect Output Device signal.

### ABSOLUTE SEARCH LEFT STATION

NOTE: The Right Station does NOT have to be loaded.

#### A. OUTPUT TO DEVICE 2 P.S.

1. I-2 of Output P.S. = MT Cde (Dev Cde 2)↑ & Sel Opt Dev↑ = Sch Lf sets = Prog Sch Op↑
2. I-5, B1-4 & B5-8 = Reset & Load Output Lats to value desired
3. Output 8 being down = Incr Sch stays down = Absolute Sch stays up
4. I-5, B13-16 = Bsy sets = Rdy resets
5. Bsy & Prog Sch Op = Prog Sch↑ = Sch In Prog↑ = Err Lite TM↑ = Err lite on
6. Prog Sch & Absol Sch = Rev Motn sets = Lf PP can't come up
7. Prog Sch & Sch Lf = Trf Sch Sta TM↑ = Trf Sch Sta sets
8. Trf Sch Sta & 10 Ct & -MT RD & Home = Sta RT resets = Sta Lf↑
9. Rev Motn & Sch Lf = Dnt Lf & Hi Bias Lf picks

#### B. TAPE REWINDS

1. Rew Sen Sw = Rew Sen↑ = Rewond sets
2. Rewond = Rev Motn resets = Sch↑ & Drop Dnt Lf & Hi Bias Lf & Pick Lf PP  
NOTE: 14 Ct is NOT used to search the Lf Station.

#### C. TAPE STOPS

1. Sch & -MT RD = Sch Pos Mag can't pick
2. Sch & -MT RD & Home = pick Cy Cl

#### D. LATCH HEAD OUT

1. Sch Pos Cont = Sch Pos↑
2. Sch Pos & -Manual Sch = Sch Pos TM↑ = MT Ctr A Rst TM↑ = MT Ctr A↓ = 10 Ct↓
3. Sch Pos TM & -Dnt Out = Fwd Motn sets = Ld Sch Sol picks = Ld Sch Sol Sw↑
4. Ld Sch Sol Sw & Sta Lf & Sch Pos TM & Trf Sch Sta = Dnt Lf picks

#### E. TAPE MOVES WITH PRESSURE PAD UP

1. Bit sensed in ctr channel = Sch Bit↑ (300 u sec) = MT Bit↑ (10 u sec)
2. MT Bit & Sch Pos TM = MT Bit SS↑ (400 u sec)
3. approximately 7 MT Bit SS's = Ref Det↑
4. Ref Det & Prog Sch = Ref Ctr AC↑ = -Ref Ctr AC↓ = step ctrs
5. when Ctrs = value in Output Lats = Eq Ct↑
6. Eq Ct & Ref Det = Stop Sch↑ = MT RD Lat Set↑ = MT RD sets
7. MT RD & Prog Sch Op = Sch IF TM↑ = OIF\* sets = Bsy resets = Prog Sch↓
8. Prog Sch down = Trf Sch Sta TM↓
9. MT RD & Sta Lf = Trf Sch Sta Resets = Sch↓  
NOTE: MT RD keeps Err lite on & Sch In Prog up.
10. MT RD = Fwd Motn resets
11. -MT RD down = drop Dnt & Ld Sch Sol & Pick Sch Pos Mag

#### F. TAPE STOPS AND HEAD SLIDE GOES HOME

1. Sch Pos down = Sch Pos TM↓ = MT Ctr A Rst TM↓
2. MT RD & -Dnt Out & Home = Set 0↑ = reset Data Lats
3. -Sch Pos TM & -10 Ct & Sta Lf = pick Cy Cl

#### G. FIRST CYCLE

1. MT RD & 10 Ct = Incr sets = step tape each cycle (Home = Incr resets)
2. MT RD & 10 Ct = pick Cy Cl

#### H. 2nd AND SUCCESSIVE CYCLES

1. MT RD & -Dnt Out & Home = Set 0↑ = reset Data Lats each cycle

#### I. 3 BIT SENSED

1. DL 3 & -DL 6 & 10 Ct (ILD P. 0301) = Car Rtn↑ = MT RD resets
2. MT RD down = don't repick Cy Cl or reset Data Lats
3. MT RD down also = Err Lite↓ & Sch In Prog↓ & Sch IF TM↓
4. -Sch IF TM = OIF\* resets = Rdy sets

Absolute Search left ends with Sch Lf, Prog Sch OP, Rewond & Eq Count all up. They will go down with the next Deselect Output Device signal.

## INCREMENTAL SEARCH

An Incremental Search is normally initiated by a Tape Search Code. It can be initiated at the Control Panel by keying in the following:

1. Forward - Key 1,9,3; station desired (or both) & Start.
2. Reverse - Key 1,2,9; station desired (or both) & Start.

NOTE: Increase the number by ONE for each additional increment desired.

Regardless of how the Search operation is initiated, it is caused by an Output to the Reader P.S. If BOTH is answered at the Control Panel, two P.S.s will be performed and the Right Station will always be searched FIRST. The tape(s) will search the increment(s) desired WITHOUT first rewinding the tape(s).

Because of the "Unload Was Last Function" flip latch, a Program Search cannot follow unloading one of the tapes.

## INCREMENTAL FORWARD SEARCH, RIGHT STATION

### A. OUTPUT TO DEVICE 6 P.S.

1. I-2 of Output P.S. = Dev Cde 6↑ & Sel Opt Dev↑ = Sch Rt sets = Prog Sch Op↑
2. I-5, B1-4 & B5-8 = Reset & Ld Output latches 7 & 8 + Increment desired  
NOTE: Output 7 = Output 7 TM↑
3. Prog Sch Op & Out 8 = Incr Sch↑ = Absolute Sch↓
4. I-5, B13-16 = Bsy sets = Rdy resets
5. Bsy & Prog Sch Op = Prog Sch↑ = Sch In Prog↑ = Err Lite TM↑ = lite on
6. Prog Sch & Sch Rt = -Sta Lf TM↑ = Sta Rt sets = Sta Lf↓ = Lf PP down = Rt PP picks
7. Prog Sch & -MT RD = Sch↑ = Sch Pos Mag can't pick
8. Sch & -MT RD & Home = pick Cy Cl

### B. LATCH HEAD OUT

1. Sch Pos Cont = Sch Pos↑
2. Sch Pos & -Manual Sch = Sch Pos TM↑
3. Sch Pos TM & Prog Sch & Incr Sch & Out 7 TM = Fwd Motn sets
4. Fwd Motn & Sch Rt = Sch Key TM↑ = Set 14↑ = 14 Ct↑
5. Fwd Motn & Sch Pos TM & -MT RD = Ld Sch Sol picks = Ld Sch Sol Sw↑
6. Ld Sch Sol Sw & 14 Ct = Dnt Rt picks

### C. TAPE MOVEMENT WITH THE PRESSURE PAD UP

1. Bits sensed in Ctr channel = Sch Bit↑ (300 u sec) = MT Bit↑ (10 u sec)
2. MT Bit & Sch Pos TM = MT Bit SS↑ (400 u sec)
3. approximately 7 MT Bit SS's = Ref Det↑
4. Ref Det & Prog Sch = Ref Ctr AC↑ = -Ref Ctr AC↓ = step Ctrs
5. when Ctrs = increment in Output Lats = Eq Ct↑
6. Eq Ct & Ref Det = Stop Sch↑ = MT Rd Lat Set↑ = MT RD sets
7. MT RD & Prog Sch Op = Sch IF TM↑ = OIF\* sets = Bsy resets = Prog Sch↓
8. -MT RD down = drop Dnt Rt & Ld Sch Sol & pick Sch Pos Mag

### D. TAPE STOPS AND HEAD SLIDE GOES HOME

1. Sch Pos down = Sch Pos TM↓
2. MT RD = Fwd Motn resets = Sch Key TM↓ = Set 14↓
3. MT RD & -Dnt Out & Home = Set 0↑ = reset Data Lats & 14 Ct↓ = Sch↓  
NOTE: MT RD keeps Err lite on & Sch In Prog up
4. -Sch Pos TM & -10 Ct & Sta Rt = pick Cy Cl

### E. FIRST CYCLE

1. MT RD & 10 Ct = Incr sets = step tape each cycle (Home = Incr resets)
2. MT RD & 10 Ct = pick Cy Cl

### F. 2nd AND SUCCESSIVE CYCLES

1. MT RD & Home = Set 0↑ = reset Data Lats each cycle

### G. 3 BIT SENSED

1. DL 3 & -DL 6 & 10 Ct (ILD P. 0301) = Car Rtn↑ = MT RD resets
2. MT RD down = don't repick Cy Cl or reset Data Lats
3. MT RD down also = Err Lite off & Sch In Prog↓ & Sch IF TM↓
4. -Sch IF TM = OIF\* resets = Rdy sets

Incremental Sch Fwd, Right Station ends with Sch Rt, Prog Sch Op, Eq Ct & Incr Sch all up. They will go down with the next Deselect Output Device signal.

## INCREMENTAL FORWARD SEARCH, LEFT STATION

### A. OUTPUT TO DEVICE 2 P.S.

1. I-2 of Output P.S. = MT Code (Device Code 2)↑ & Sel Opt Dev↑ = Sch Lf sets = Prog Sch Op↑
2. I-5, B1-4 & B5-8 = Reset & Ld Output Lats 7 & 8 + Increment desired  
NOTE: Output 7 = Output 7 TM↑
3. Prog Sch Op & Out 8 = Incr Sch↑ = Absolute Sch↓
4. I-5, B 13-16 = Bsy sets = Rdy resets
5. Bsy & Prog Sch Op = Prog Sch↑ = Sch In Prog↑ = Err Lite TM↑ = lite on
6. Prog Sch & -MT RD = Sch↑
7. Prog Sch & Sch Lf = Trf Sch Sta TM↑ = Trf Sch Sta sets
8. Trf Sch Sta & 10 Ct & -MT RD & Home = Sta Rt resets = Sta Lf↑
9. Sta Lf = Lf PP picks
10. Sch & -MT RD = Sch Pos Mag can't pick
11. Sch & -MT RD & Home = pick Cy Cl

### B. LATCH HEAD OUT

1. Sch Pos Cont = Sch Pos↑
2. Sch Pos & -Manual Sch = Sch Pos TM↑
3. Sch Pos TM & Sch Lf = Mt Ctr A Rst TM↑ = Mt Ctr A resets = 10 Ct↓
4. Sch Pos TM & Prog Sch & Incr Sch & Out 7 TM = Fwd Motn sets
5. Fwd Motn & Sch Pos TM & -MT RD = Ld Sch Sol picks = Ld Sch Sol Sw↑
6. Ld Sch Sol Sw & Sta Lf & Sch Pos TM & Trf Sch Sta = Dnt Lf picks

### C. TAPE MOVEMENT WITH THE PRESSURE PAD UP

1. Bit sensed in Ctr channel = Sch Bit↑ (300 u sec) = MT Bit↑ (10 u sec)
2. MT Bit & Sch Pos TM = MT Bit SS↑ (400 u sec)
3. approximately 7 MT Bit SS's = Ref Det↑
4. Ref Det & Prog Sch = Ref Ctr AC↑ = -Ref Ctr AC↓ = step Ctrs
5. when Ctrs = Increment in Output Lats = Eq Ct↑
6. Eq Ct & Ref Det = Stop Sch↑ = MT RD Lat Set↑ = MT RD sets
7. MT RD & Prog Sch Op = Sch IF TM↑ = OIF\* sets = Bsy resets = Prog Sch↓ = Trf Sch Sta TM↓
8. MT RD & Sta Lf = Trf Sch Sta resets = Sch↓  
NOTE: MT RD keeps Err lite on & Sch In Prog up
9. -MT RD down = drop Dnt Lf & Ld Sch Sol & pick Sch Pos Mag

### D. TAPE STOPS AND HEAD SLIDE GOES HOME

1. Sch Pos down = Sch Pos TM↓ = Mt Ctr A Rst TM↓
2. MT RD = Fwd Motn resets
3. MT RD & -Dnt Out & Home = Set 0↑ = reset Data Lats
4. -Sch Pos TM & -10 Ct & Sta Lf = pick Cy Cl

### E. FIRST CYCLE

1. MT RD & 10 Ct = Incr sets = step tape each cycle (Home = Incr resets)
2. Mt Rd & 10 Ct = pick Cy Cl

### F. 2nd AND SUCCESSIVE CYCLES

1. MT RD & Home = Set 0↑ = reset Data Lats each cycle

### G. 3 BIT SENSED

1. DL 3 & -DL 6 & 10 Ct (ILD P.0301) = Car Rtn↑ = MT RD resets
2. MT RD down = don't repick Cy Cl or reset Data Lats
3. MT RD down also = Err lite off & Sch In Prog↓ & Sch IF TM↓
4. -Sch IF TM = OIF\* resets = Rdy sets

Incremental Search Fwd, Left Station ends with Sch Lf, Prog Sch Op, Eq Ct and Incr Sch all up. They will go down with the next Deselect Output Device signal.

**INCREMENTAL REVERSE SEARCH, RIGHT STATION****A. OUTPUT TO DEVICE 6 P.S.**

1. I-2 of Output P.S. = Device Cde 6↑ & Sel Opt Dev↑ = Sch Rt sets = Prog Sch Op↑
2. I-5, B1-4 & B5-8 = Reset & Ld Output Lat 8 + incr desired (excluding Out 7)
3. Prog Sch Op & Out 8 = Incr Sch↑ = Absolute Sch↓
4. Incr Sch & -Out 7 TM & Ld Opt Lat = Inh Stop Sch sets
5. I-5, B13-16 = Bsy sets = Rdy resets
6. Bsy & Prog Sch Op = Prog Sch↑ = Sch In Prog↑ = Err Lite TM↑ = lite on
7. Prog Sch & Sch Rt = -Sta Lf Tm↑ = Sta Rt sets = Sta Lf↓ = Lf PP drops = Rt PP picks
8. Prog Sch & -MT RD = Sch↑ = Sch Pos Mag can't pick
9. Sch & -MT RD & Home = pick Cy Cl

**B. LATCH HEAD OUT**

1. Sch Pos Cont = Sch Pos↑ = Sch Pos TM↑
2. Sch Pos TM & Incr Sch & -Out 7 TM & Prog Sch = Rev Motn sets
3. Rev Motn & Sch Rt = Mt Ctr A Rst TM↑ = Mt Ctr A resets = 10 Ct↓
4. Rev Motn & Sch Rt = Dnt Rt & Hi Bias Rt picks

**C. TAPE MOVES IN REWIND DIRECTION WITH PRESSURE PAD UP**

1. Bits Sensed in Ctr channel = Sch Bit↑ (300 u Sec) = MT Bit↑ (10 u sec)
2. MT Bit & Sch Pos TM = MT Bit SS↑ (400 u sec)
3. approximately 7 MT Bit SS's = Ref Det↑
4. Ref Det & Prog Sch = Ref Ctr AC↑ = -Ref Ctr AC↓ = step Ctrs
5. when Ctrs equal increment in Output Lats = Eq Ct↑
6. Eq Ct & Ref Det = Stop Sch↑ (Ref Det↓ = Stop Sch↓)  
NOTE: MT RD Lat Set stays down because -Inh Stop Sch is down
7. Eq Ct & Incr Sch = Rewound sets = Rev Motn resets = drop Dnt, Hi Bias & Mt Ctr A Rst TM↓

**D. TAPE STOPS BUT HEAD DOES NOT UNLATCH**

1. Rewound & -Dnt Out = Fwd Motn sets = Sch Key TM↑ = Set 14↑ = 14 Ct↑
2. Fwd Motn = Ld Sch Sol picks = Ld Sch Sol Sw↑
3. Ld Sch Sol Sw & 14 Ct = Dnt Rt picks = Sch shoe on spring clutch

**E. TAPE REVERSES DIRECTION (OVER SAME REF CODE)**

1. one Bit sensed in Ctr Channel = Sch Bit↑ = MT Bit↑
2. MT Bit & Incr Sch & Ld Sch Sol Sw = MT RD Lat Set↑ = MT RD sets
3. MT Bit & Incr Sch & Ld Sch Sol Sw = Inh Stop Sch resets  
NOTE: Since the first Bit stops the Search, the Ctr will not step.
4. MT Rd & Prog Sch Op = Sch IF TM↑ = OIF\* sets = Bsy resets = Prog Sch↓
5. -MT RD down = drop Dnt Rt & Ld Sch Sol & pick Sch Pos Mag

**F. TAPE STOPS AND THE HEAD SLIDE GOES HOME**

1. Sch Pos down = Sch Pos TM↓
2. MT RD = Fwd Motn resets = Sch Key TM↓ = Set 14↓
3. MT RD & -Dnt Out & Home = Set 0↑ = reset Data Lats & 14 Ct↓ = Sch↓  
NOTE: MT RD keeps Err lite on & Sch In Prog up
4. -Sch Pos Tm & -10 Ct & Sta Rt = pick Cy Cl

**G. FIRST CYCLE**

1. MT RD & 10 Ct = Incr sets = step tape each cycle (Home = Incr resets)
2. MT RD & 10 Ct = pick Cy Cl

**H. 2nd AND SUCCESSIVE CYCLES**

1. MT RD & Home = Set 0↑ = reset Data Lats each cycle

**I. 3 BIT SENSED**

1. DL 3 & -DL 6 & 10 Ct (ILD P. 0301) = Car Rtn↑ = MT RD resets
2. MT RD down = don't repick Cy Cl or reset Data Lats
3. MT RD down also = Err lite off & Sch In Prog↓ & Sch IF TM↓
4. -Sch IF TM = OIF\* resets = Rdy sets

Incremental Reverse Search, Right Station ends with Sch Rt, Prog Sch Op, Incr Sch, Rewound and Eq Ct all up. They will go down with the next Deselect Output Device signal.

**INCREMENTAL REVERSE SEARCH, LEFT STATION****A. OUTPUT TO DEVICE 2 P.S.**

1. I-2 Of Otpt P.S. = MT Cde (Dev Cde 2)↑ & Sel Opt Dev↑ = Sch Lf sets = Prog Sch Op↑
2. I-5, B1-4 & B5-8 = Reset & Ld Out Lat 8 + incr desired (except Out 7)
3. Prog Sch Op & Out 8 = Incr Sch↑ = Absolute Sch↓
4. Incr Sch & -Out 7 TM & Ld Opt Lat = Inh Stop Sch sets
5. I-5, B13-16 = Bsy sets = Rdy resets
6. Bsy & Prog Sch Op = Prog Sch↑ = Sch In Prog↑ = Err Lite TM↑ = lite on
7. Prog Sch & -MT RD = Sch↑
8. Prog Sch & Sch Lf = Trf Sch Sta TM↑ = Trf Sch Sta sets
9. Trf Sch Sta & 10 Ct & -MT RD & Home = Sta Rt resets = Sta Lf↑ = Lf PP picks
10. Sch & -MT RD = Sch Pos Mag can't pick
11. Sch & -MT RD & Home = pick Cy Cl

**B. LATCH HEAD OUT**

1. Sch Pos Cont = Sch Pos↑ = Sch Pos TM↑
2. Sch Pos TM & Sch Lf = Mt Ctr A Rst TM↑ = Mt Ctr A resets = 10 Ct↓
3. Sch Pos Tm & Incr Sch & -Out 7 TM & Prog Sch = Rev Motn sets
4. Rev Motn & Sch Lf = Dnt Lf & Hi Bias picks

**C. TAPE MOVES IN REWIND DIRECTION WITH PRESSURE PAD UP**

1. Bits sensed in Ctr channel = Sch Bit↑ (300 u sec) = MT Bit↑ (10 u sec)
2. MT Bit & Sch Pos TM = MT Bit SS↑ (400 u sec)
3. approximately 7 MT Bit SS's = Ref Det↑
4. Ref Det & Prog Sch = Ref Ctr AC↑ = -Ref Ctr AC↓ = step Ctrs
5. when Ctrs equal increment in Output Lats = Eq Ct↑
6. Eq Ct & Ref Det = Stop Sch↑ (Ref Det↓ = Stop Sch↓)  
NOTE: MT RD Lat Set stays down because -Inh Stop Sch is down
7. Eq Ct & Incr Sch = Rewound sets = Rev Motn resets = drop Dnt Lf & Hi Bias

**D. TAPE STOPS BUT HEAD DOES NOT UNLATCH**

1. Rewound & -Dnt Out = Fwd Motn sets = Ld Sch Sol picks = Ld Sch Sol Sw↑
2. Ld Sch Sol Sw & Trf Sch Sta = Dnt Lf picks = Sch shoe on spring clutch

**E. TAPE REVERSES DIRECTION (OVER SAME REF CODE)**

1. one Bit sensed in ctr channel = Sch Bit↑ = MT Bit↑
2. MT Bit & Incr Sch & Ld Sch Sol Sw = MT RD Lat Set↑ = MT RD sets
3. MT Bit & Incr Sch & Ld Sch Sol Sw = Inh Stop Sch resets  
NOTE: Since the first Bit stops the Search, the Counters will not step.
4. MT RD & Prog Sch Op = Sch IF TM↑ = OIF\* sets = Bsy resets = Prog Sch↓ = Trf Sch Sta TM↓
5. MT RD & Sta Lf = Trf Sch Sta resets = Sch↓  
NOTE: MT RD keeps Err lite on & Sch In Prog up
6. -MT RD down = drop Dnt Lf & Ld Sch Sol & pick Sch Pos Mag

**F. TAPE STOPS AND HEAD SLIDE GOES HOME**

1. Sch Pos down = Sch Pos TM↓ = Mt Ctr A Rst TM↓
2. MT RD = Fwd Motn resets
3. MT RD & -Dnt Out & Home = Set 0↑ = reset Data Lats
4. -Sch Pos Tm & -10 Ct & Sta Lf = pick Cy Cl

**G. FIRST CYCLE**

1. MT RD & 10 Ct = Incr sets = step tape each cycle (Home = Incr resets)
2. MT RD & 10 Ct = Pick Cy Cl

**H. 2nd AND SUCCESSIVE CYCLES**

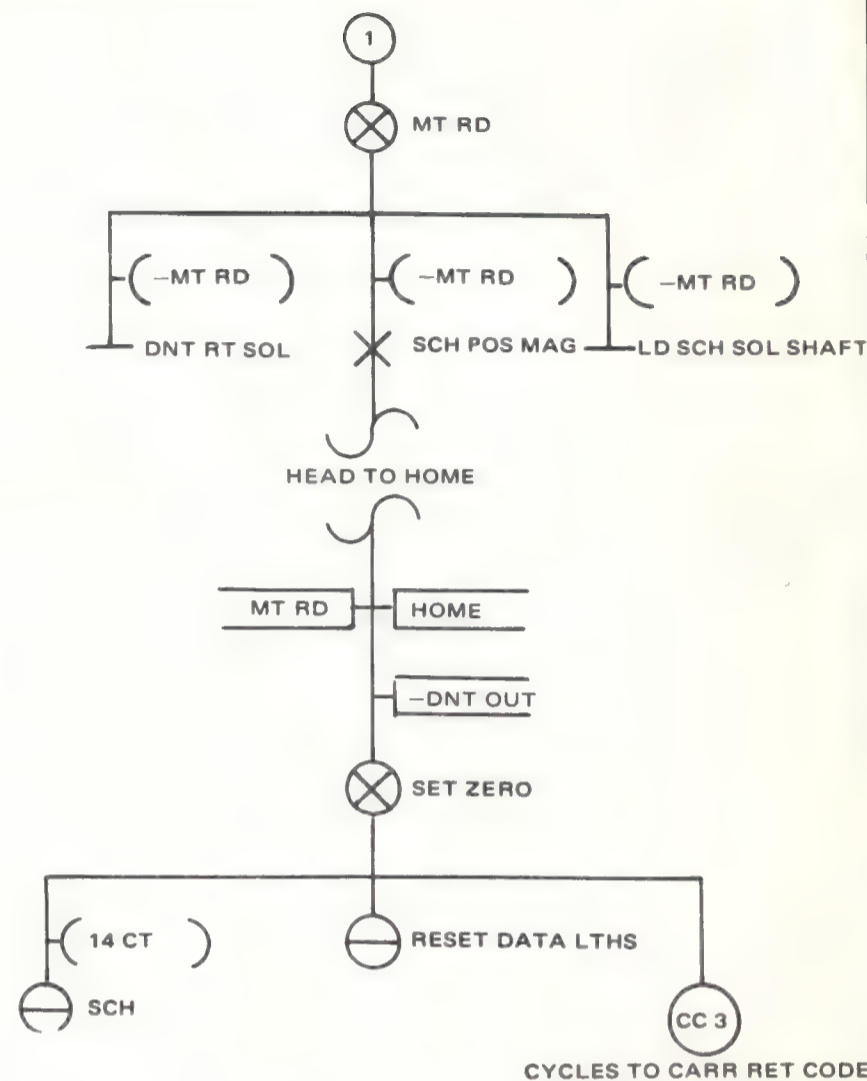
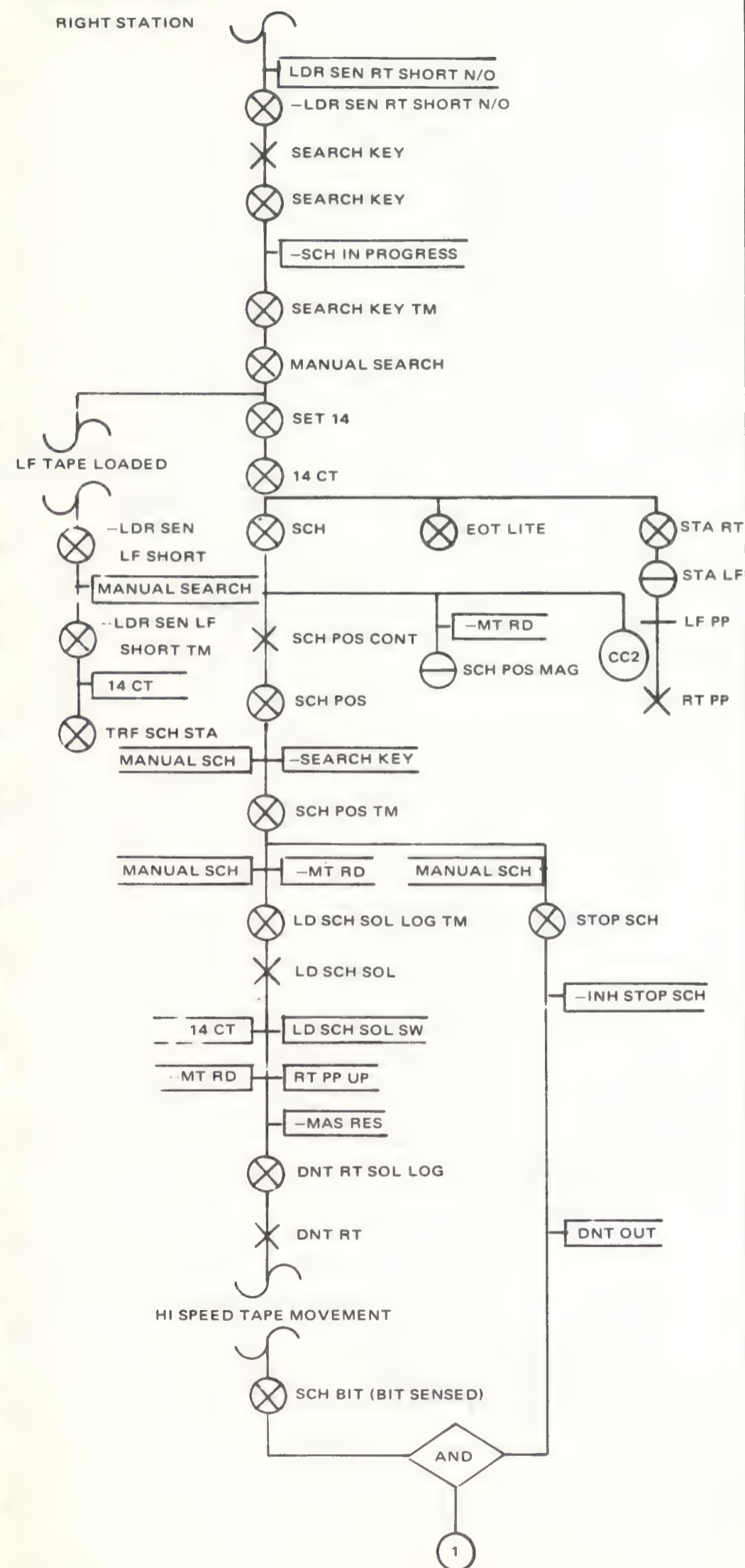
1. MT RD & Home = Set 0↑ = reset Data Lats each cycle

**I. 3 BIT SENSED**

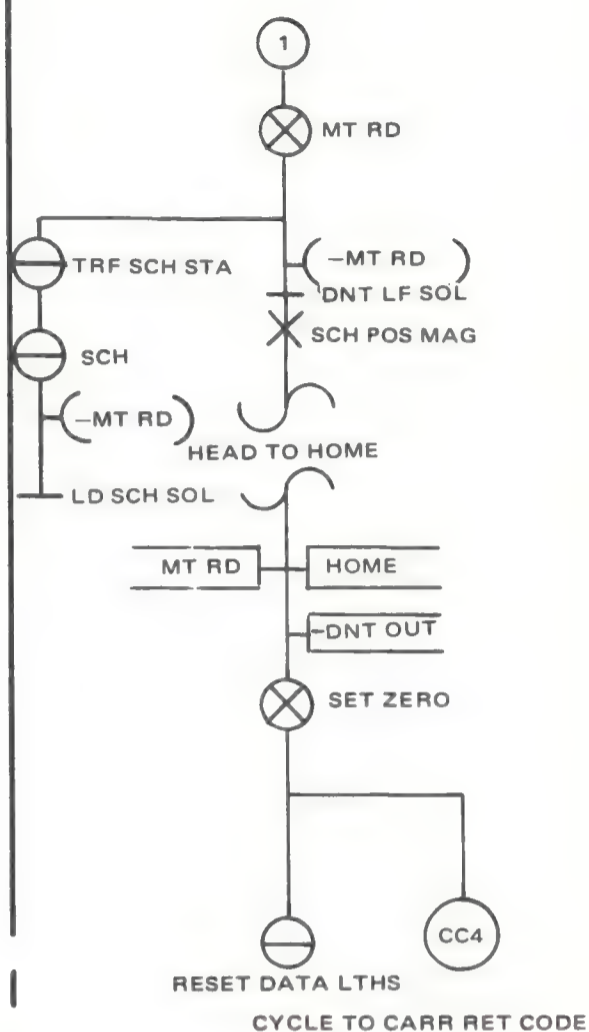
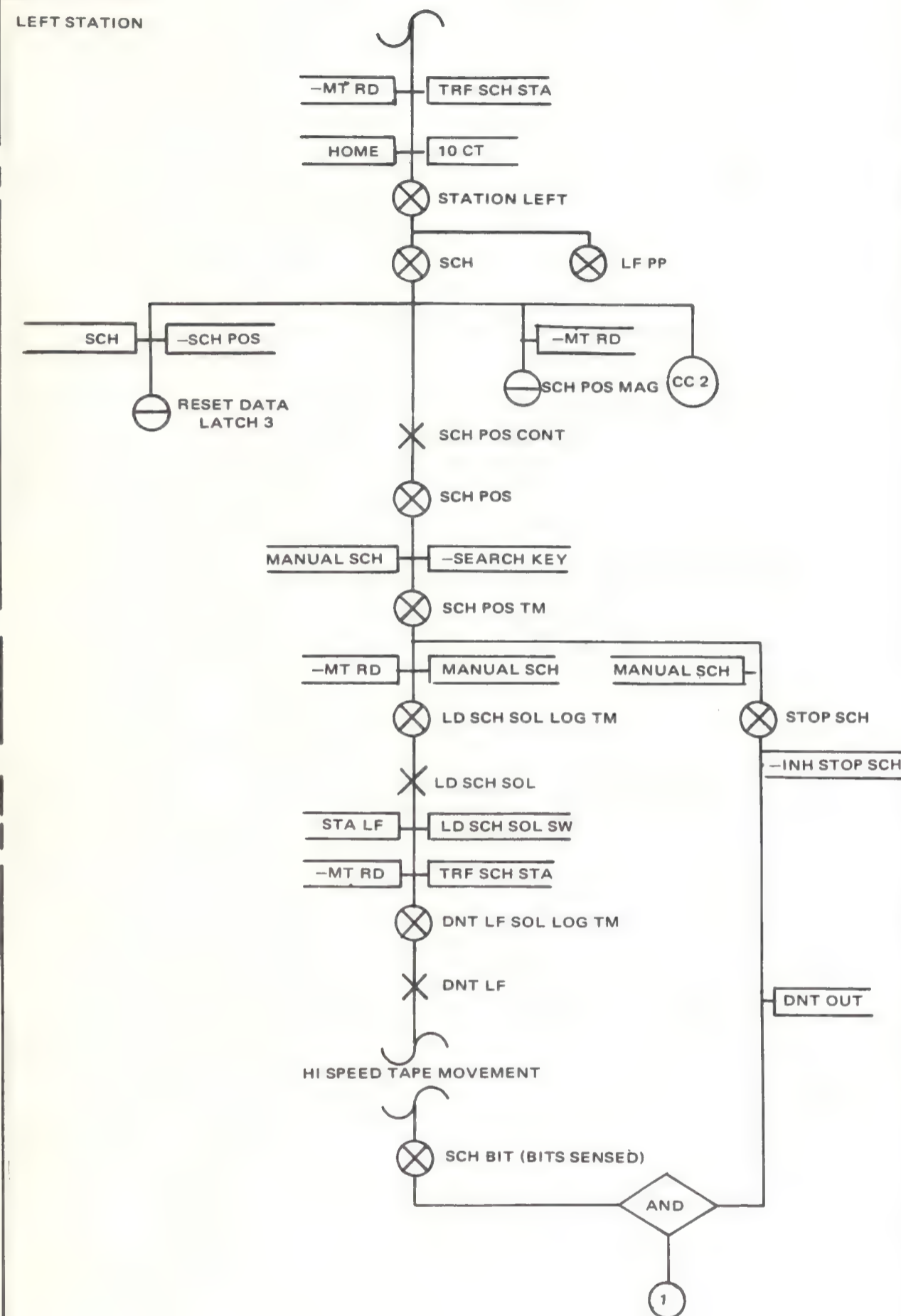
1. DL 3 & -DL 6 & 10 Ct (ILD P. 0301) = Car Rtn↑ = MT RD resets
2. MT RD down = don't repick Cy Cl or reset Data Lats
3. MT RD down also = Err lite off & Sch In Prog↓ & Sch IF TM↓
4. -Sch IF TM = OIF\* resets = Rdy sets

Incremental Reverse Search, Left Station ends with Sch Lf, Prog Sch Op, Incr Sch, Rewound & Eq Ct all up. They will go down with the next Deselect Output Device signal.

MANUAL SEARCH  
RIGHT STATION

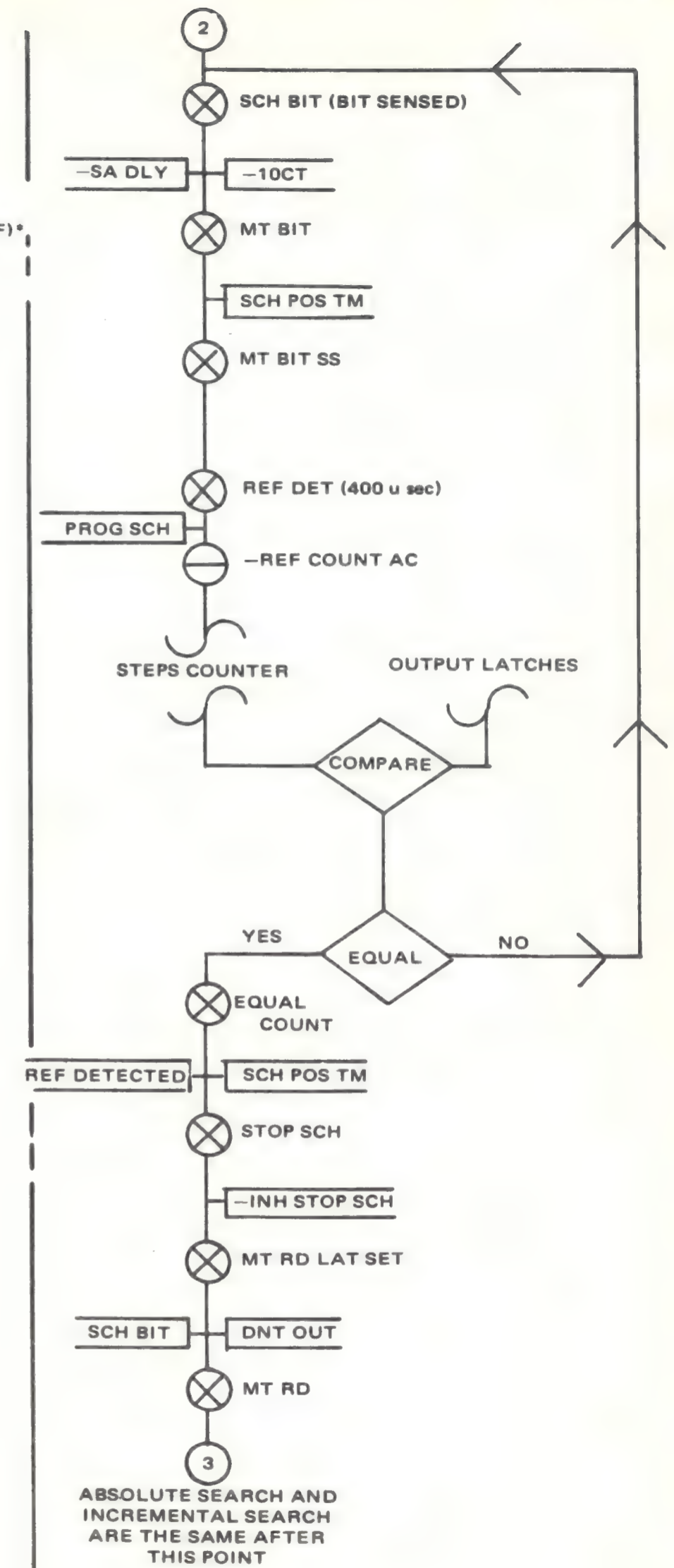
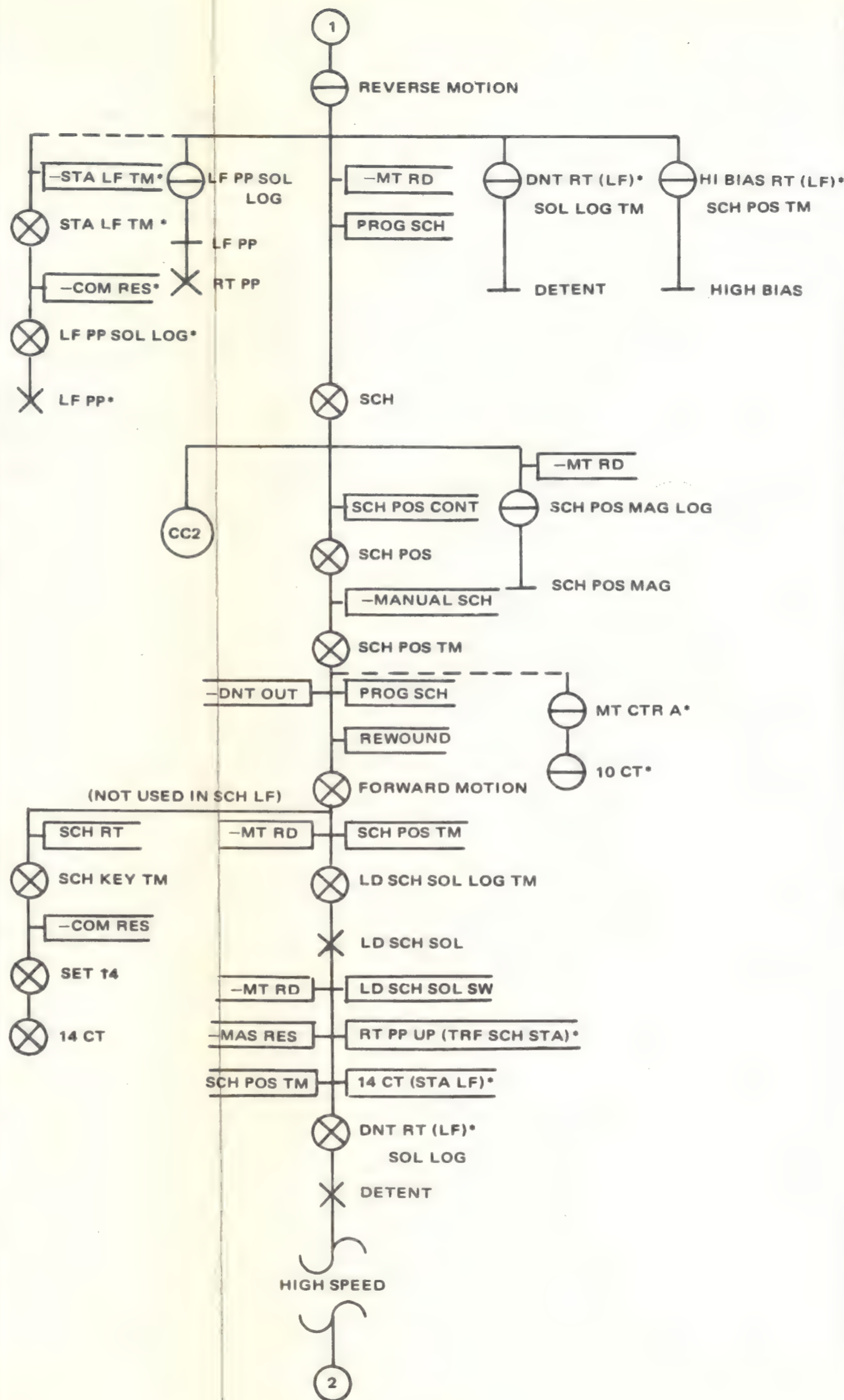
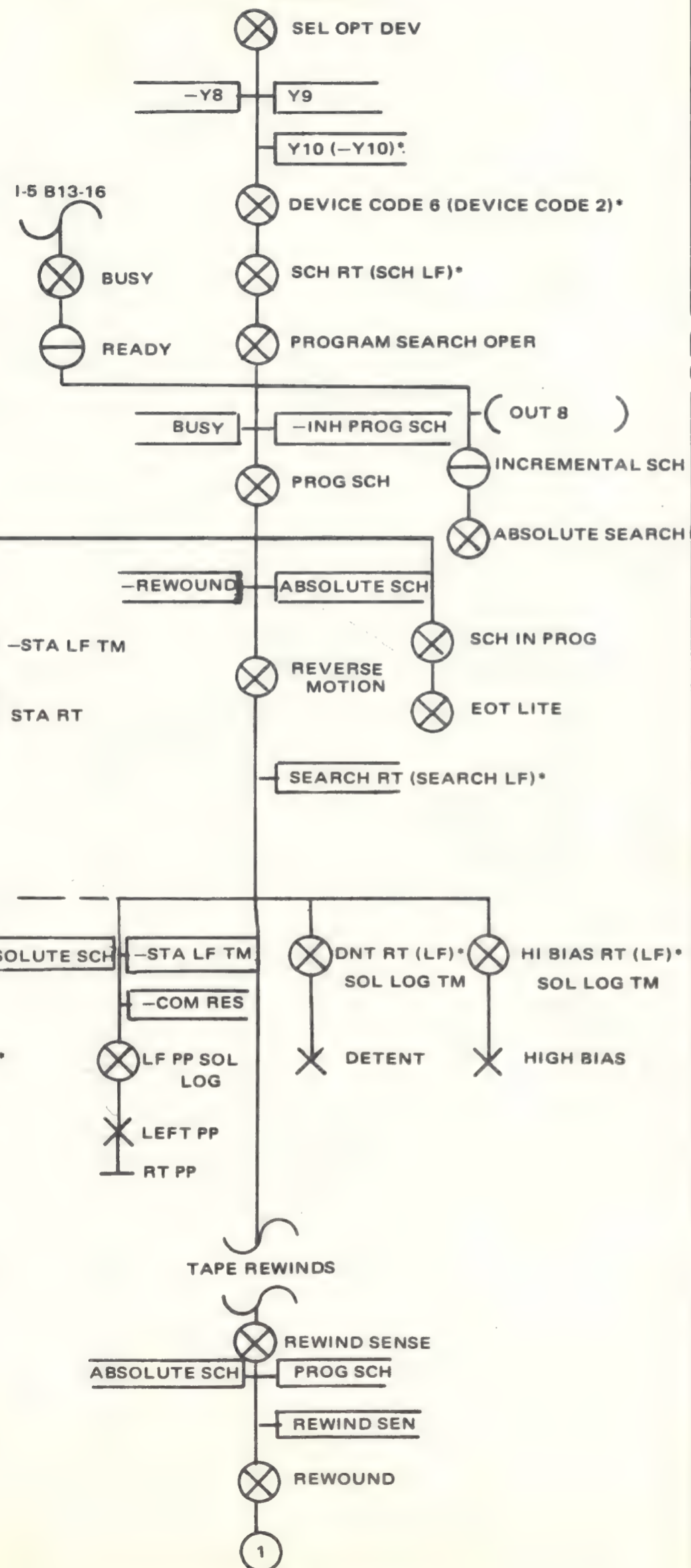


MANUAL SEARCH  
LEFT STATION



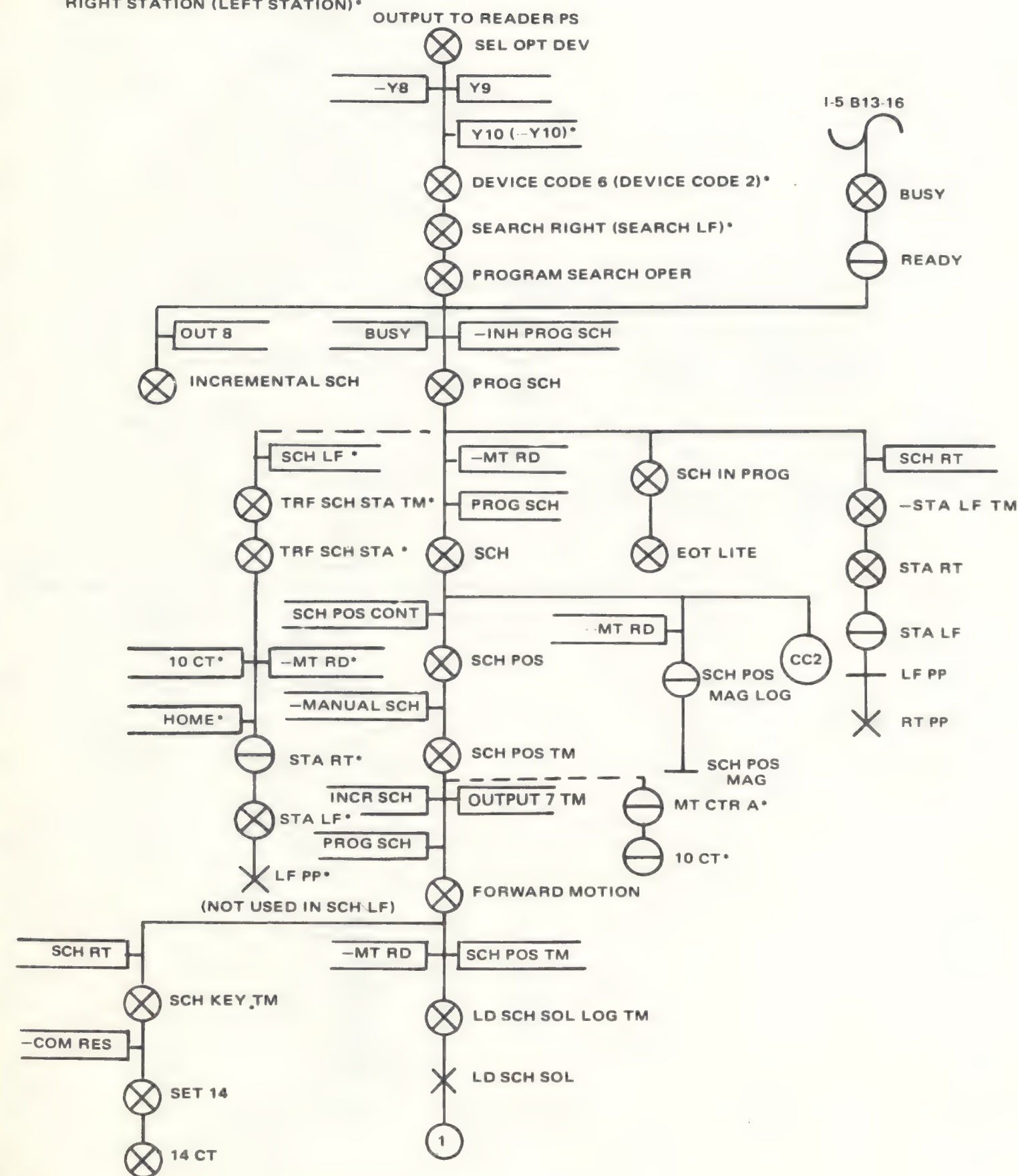
ABSOLUTE SCH  
RIGHT STATION (LEFT STATION)\*

OUTPUT TO READER P S

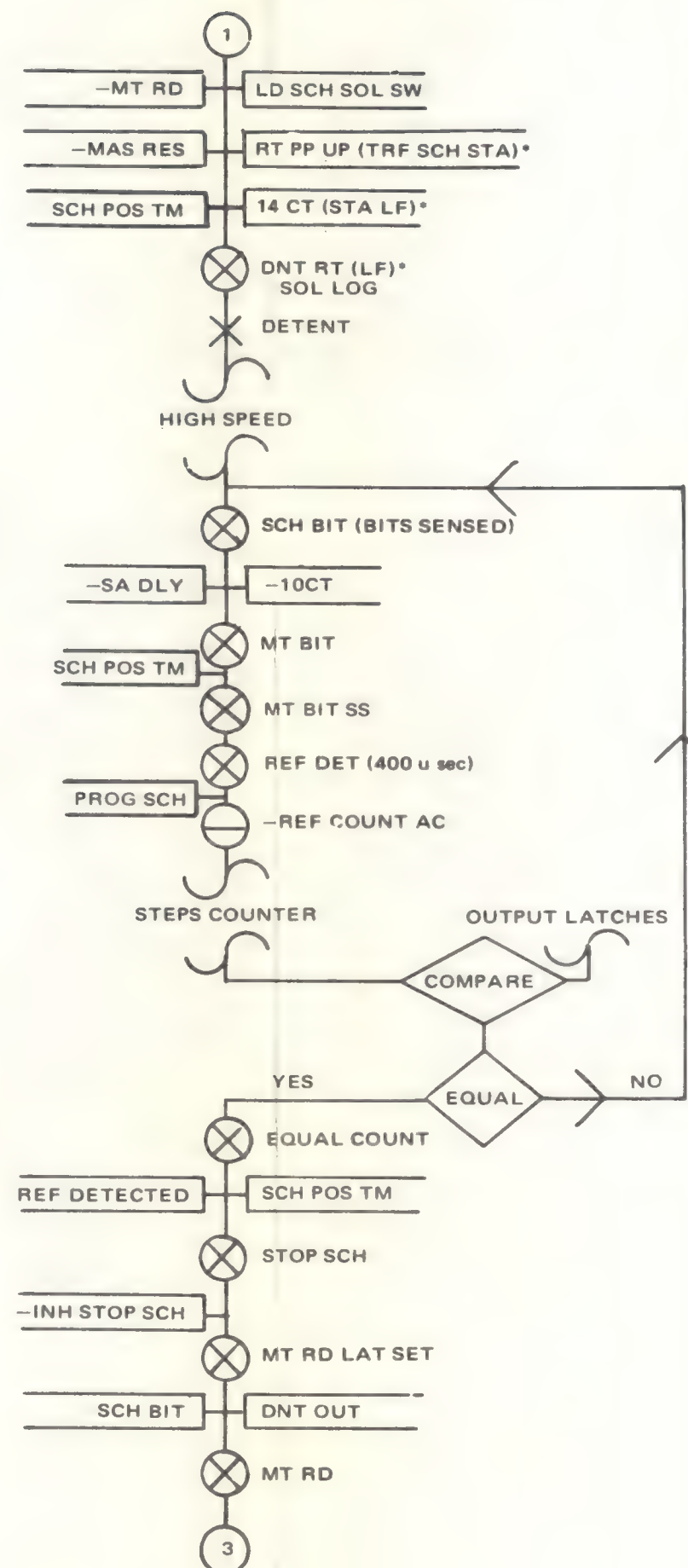


# INCREMENTAL SEARCH FORWARD

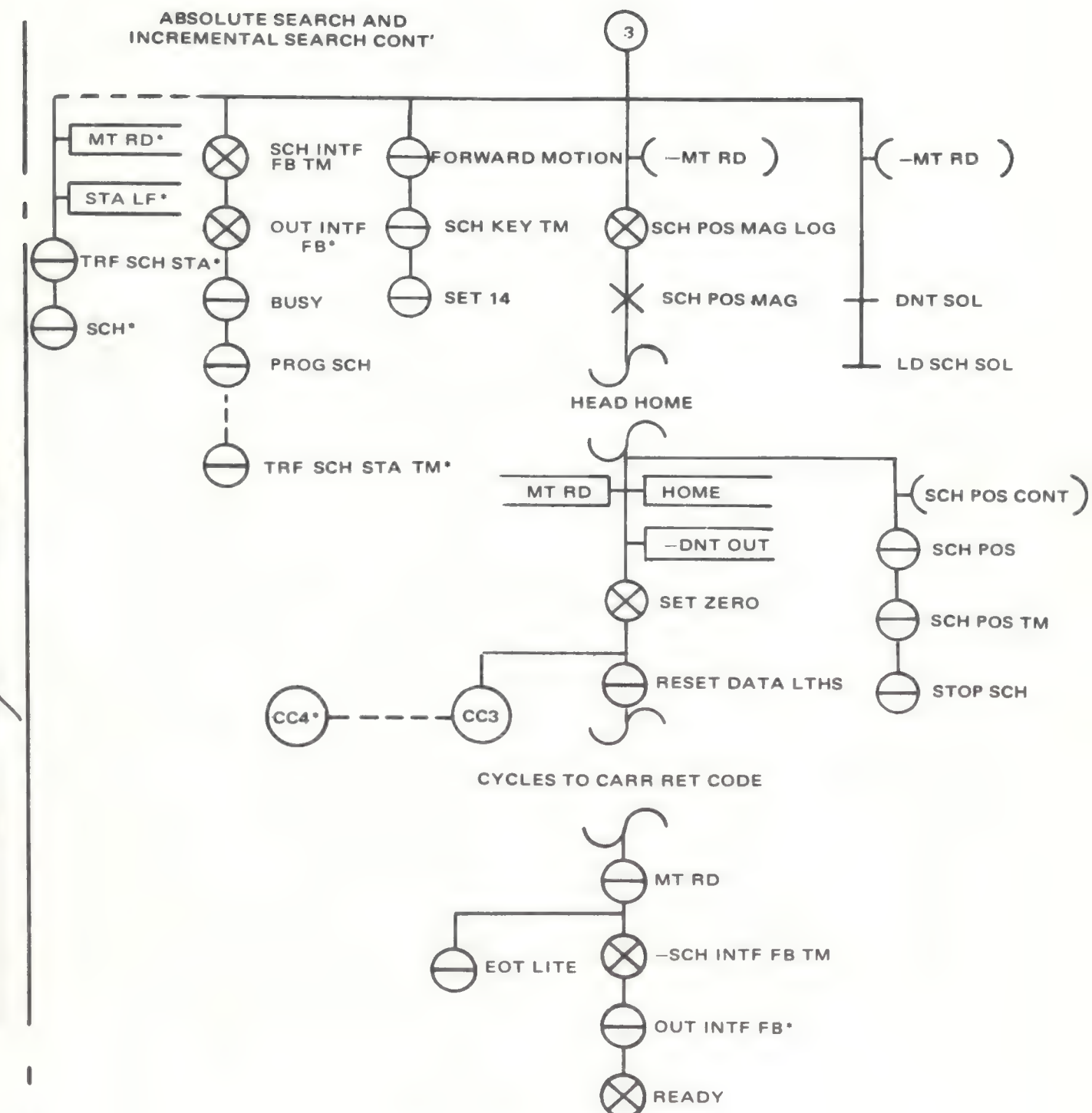
RIGHT STATION (LEFT STATION)\*



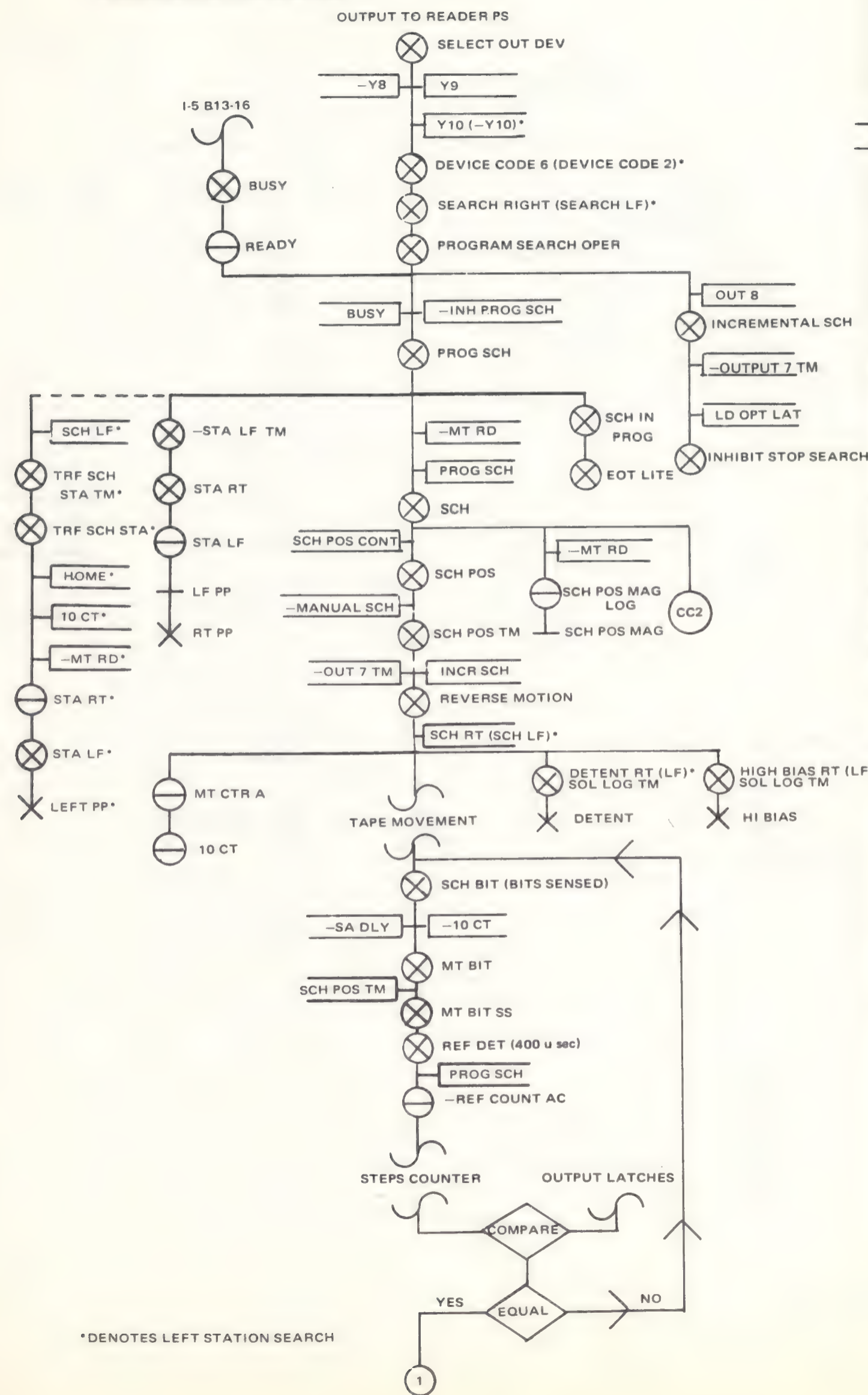
\*DENOTES LEFT STATION SEARCH



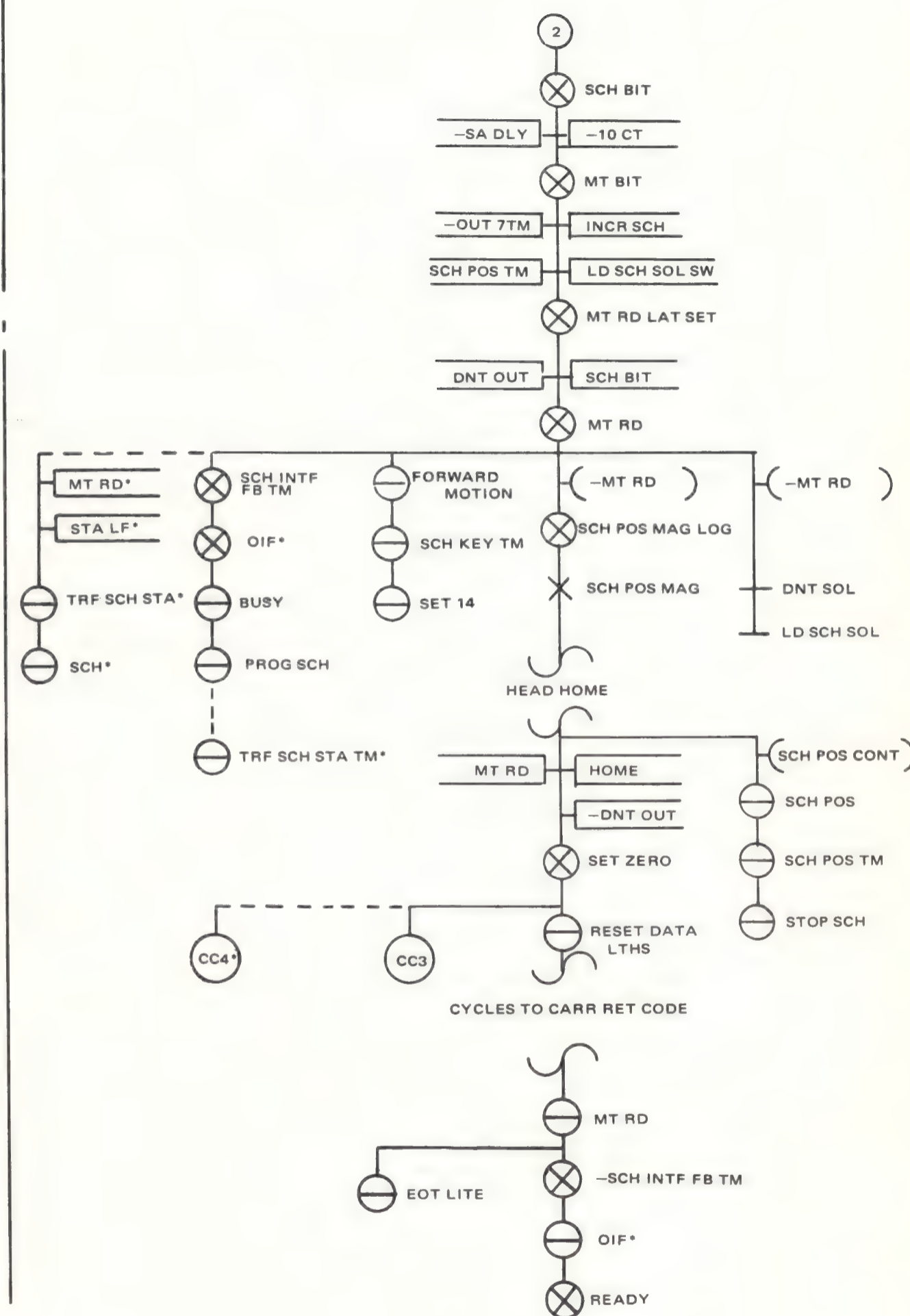
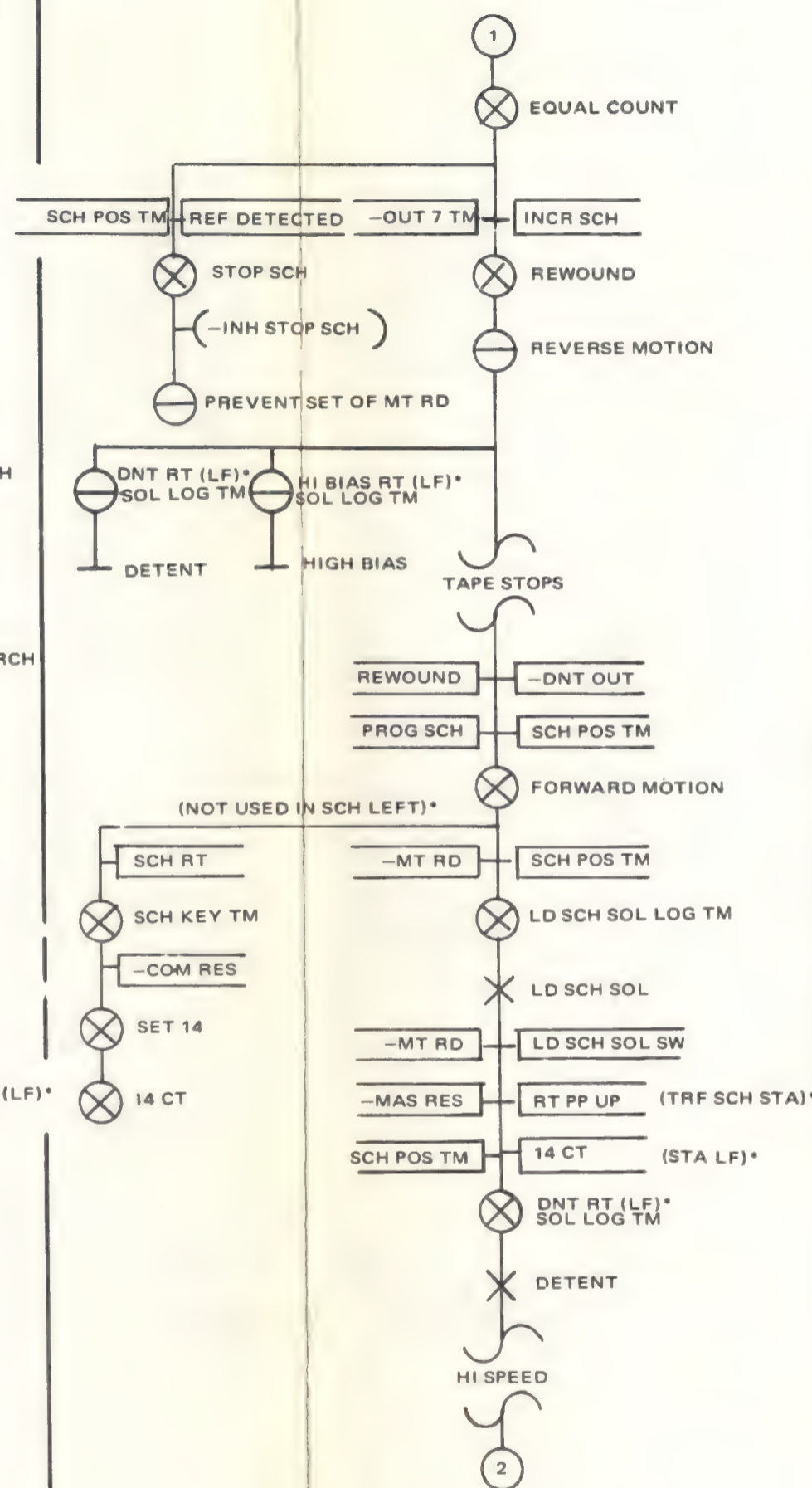
# ABSOLUTE SEARCH AND INCREMENTAL SEARCH CONT'

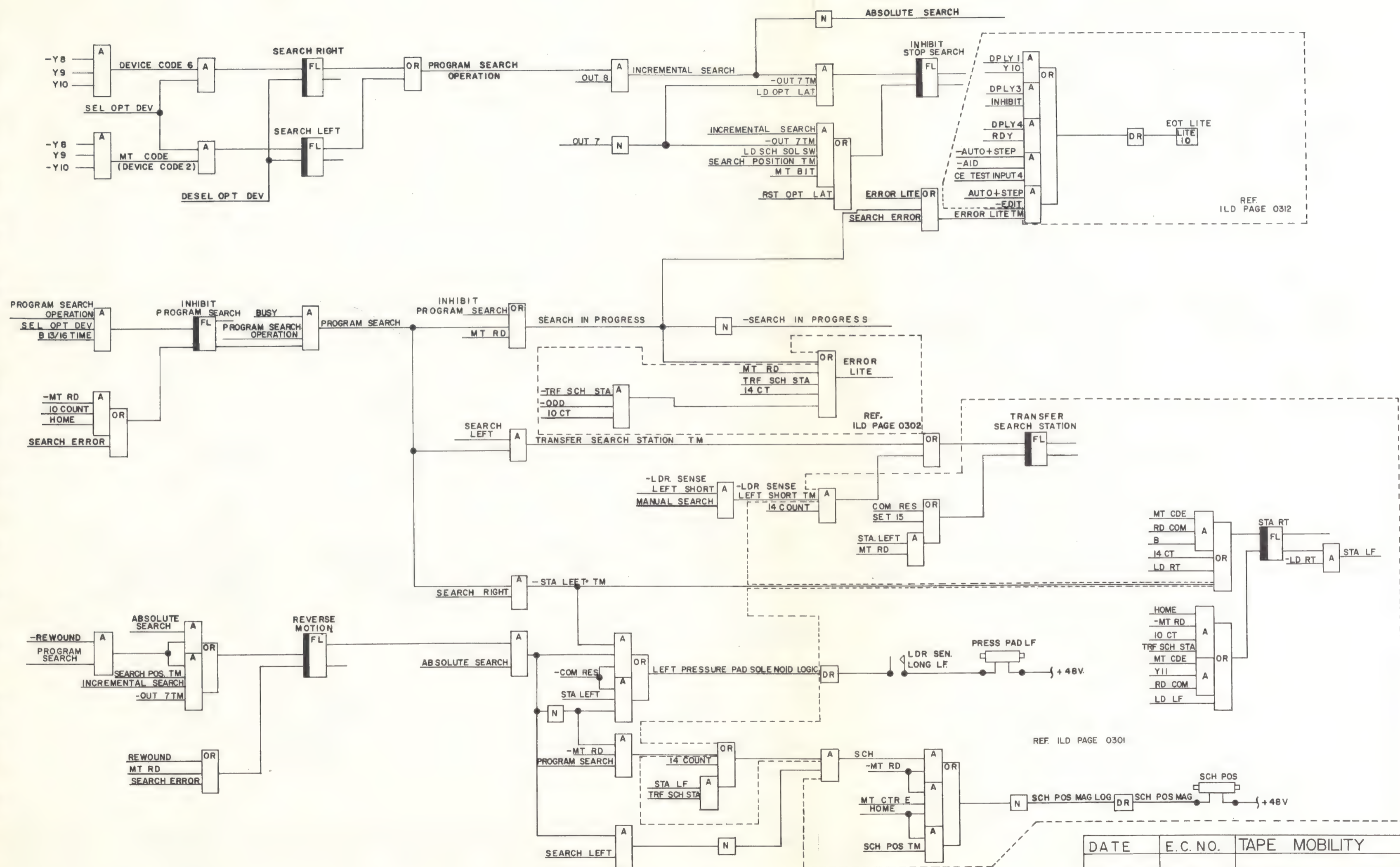


INCREMENTAL SEARCH REVERSE  
RIGHT STATION ( LEFT STATION)\*

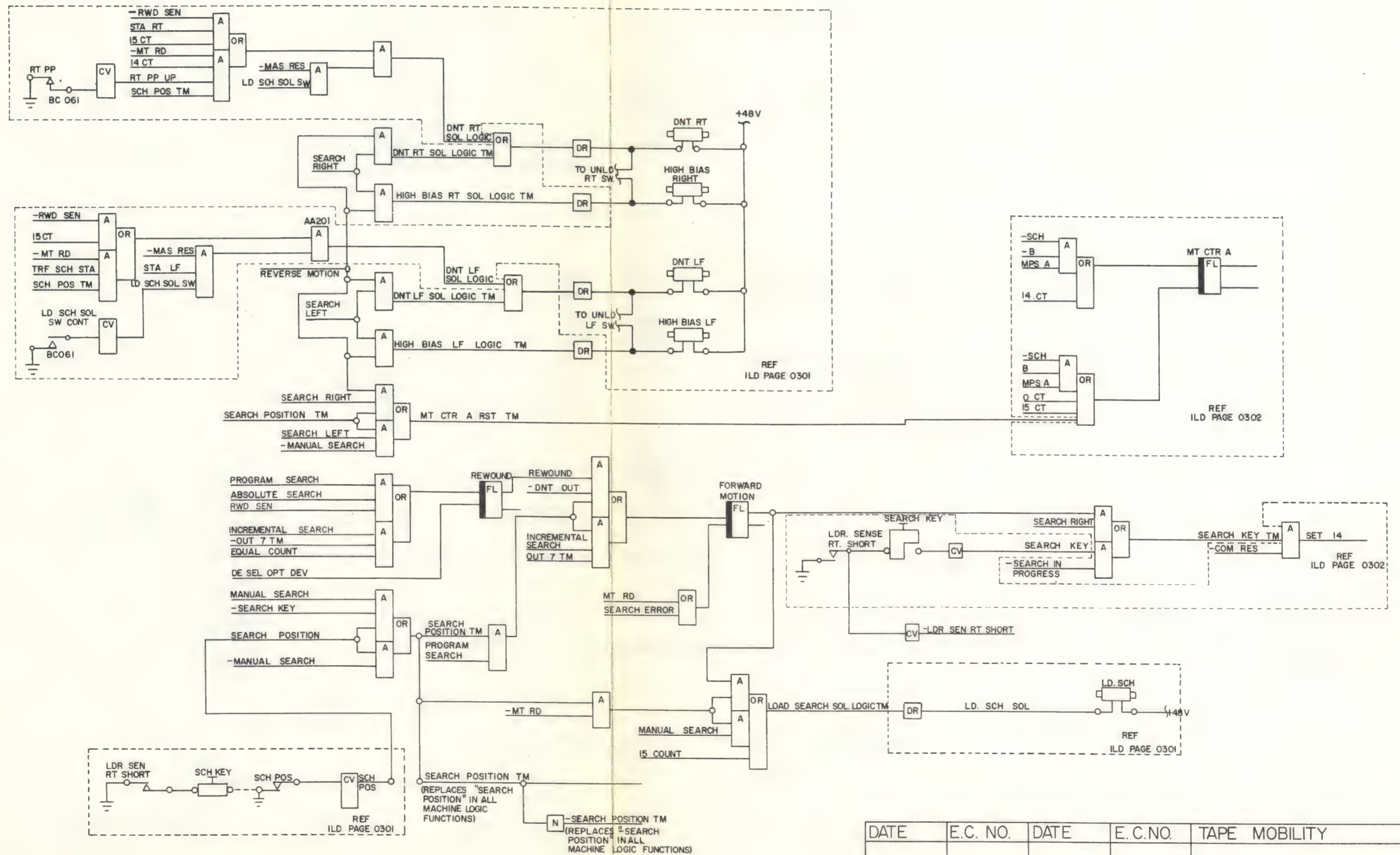


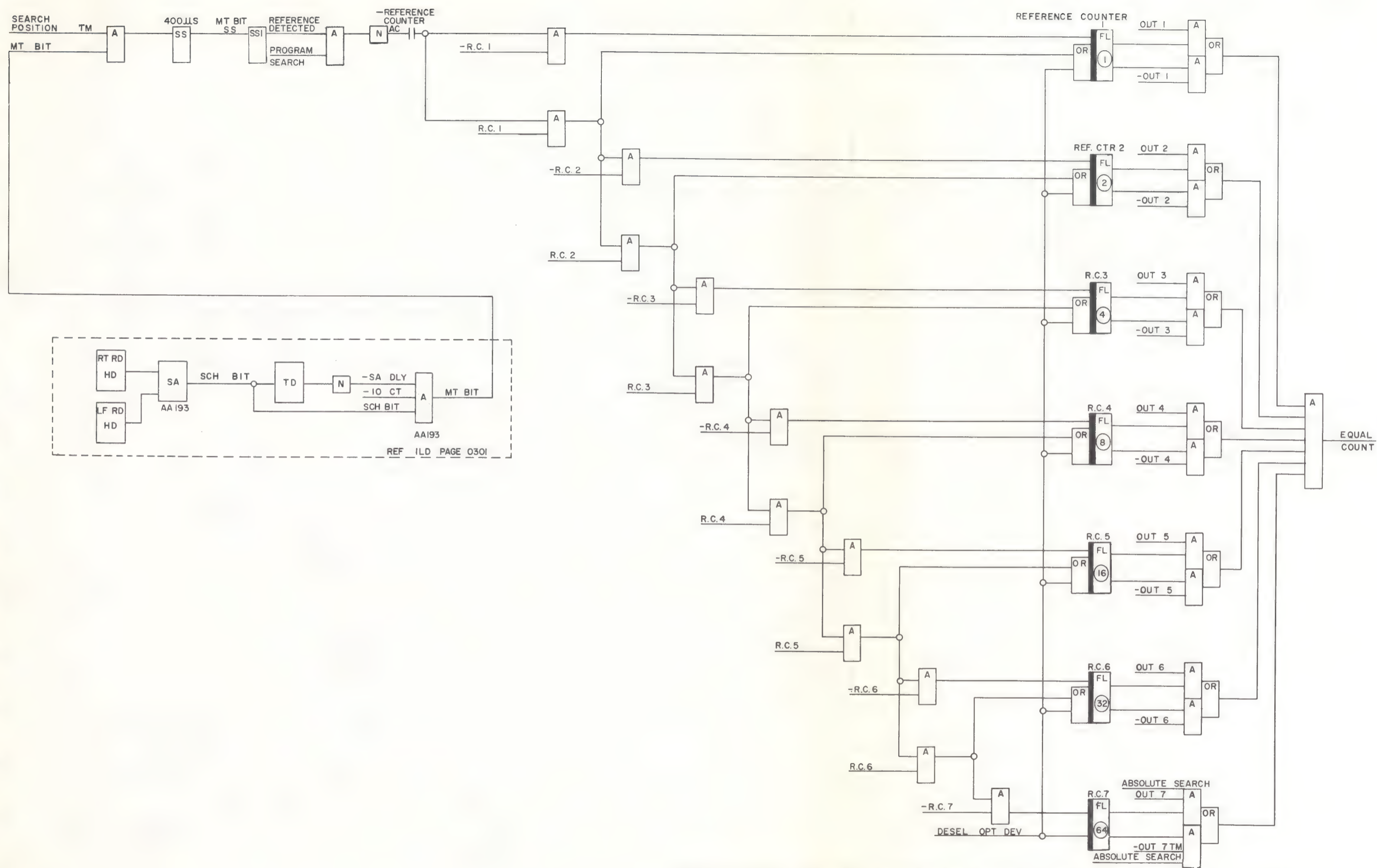
\*DENOTES LEFT STATION SEARCH



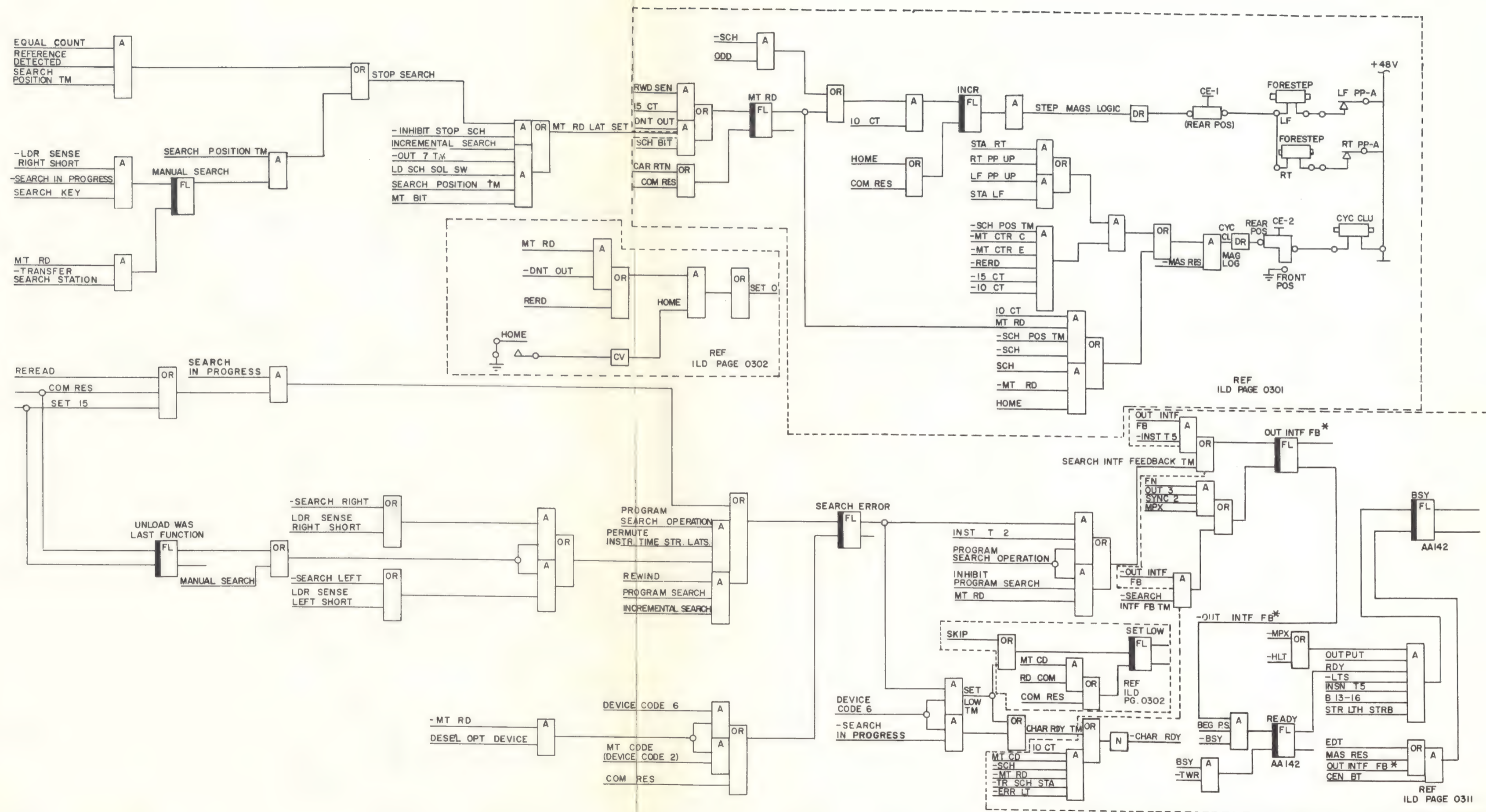


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		IBM 6310/6320	





DATE	E.C. NO.	DATE	E.C. NO.	TAPE MOBILITY	
				PART NO. 1450027	PAGE 22
				IBM 6310/6320	



DATE	E. C. NO.	DATE	E. C. NO.	TAPE MOBILITY	
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				IBM 6310/6320	

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### MT/SC WITH THIRD TAPE RECORDER

#### INTRODUCTION

The T.T.R. feature is an additional Tape Station added to the MT/SC system. Its function is to record a tape. With this feature the MT/SC system can now prepare a new tape as the Output copy is printed. A discussion of how this is accomplished will give some insight as to the applications this feature can be applied to.

When a code is read from either the original tape or the Merge tape, the PRECON dictates what should be done with this code. Some codes will be dumped, some will be sent only to the T.T.R. for recording and some will be sent to both the T.T.R. and the Printer.

Address information from the Merge Tape and lines that are merged out will be dumped.

Instructions such as type fonts or leading to be used (Preceded by a Prefix code and followed by a comma), recorded Measure, Indent and Mode codes will be sent only to the T.T.R.

Text will be sent to the T.T.R. and then the Printer, One code at the time. In the Justify Mode where C.R.'s and Spaces may need to be changed, they are supplied by the PRECON. The PRECON also supplies the codes for an End of Tape Sequence, Reference codes and Hyphenation decisions. These are discussed under their respective headings.

The customer's particular application will dictate the use of the T.T.R. as it has all our other products. It can build an updated tape from an original and Merge tape and/or change line endings (Justify Mode). Applications such as Classified ads, Catalogs, Directories and other Publications which require periodic updating can be easily handled by the MT/SC with T.T.R.

#### THIRD TAPE RECORDER

The Third Tape Feature adds an additional tape deck console to the MT/SC system. This console contains a single station tape deck, an electronic gate and a motor start relay. The T.T.R. gets its power from the C.C.U. power supply. This power supply has been modified to accommodate the heavier load. The C.C.U also has a 23K memory instead of the 16K memory.

Basically, codes recorded on the Third Tape may originate from one of the three following sources: The Original tape, the Merge tape or the PRECON.

All codes from the Original tape and/or Merge tape are recorded on the third tape, except Reference codes and codes dumped because of a Merge operation (including address information). The PRECON provides Space, Backspace, Hyphen codes (when Hyphenation decisions are made) and Reference codes to be recorded on the Third Tape. In the Justify mode, line endings on the Third Tape will match those on the MT/SC Output copy.

Discounting the codes for handling the text, it can be said that the Third Tape will always match the Hard copy.



## FUNCTIONS OF THE T.T.R.

### UNLOAD

Unload on the T.T.R. is almost identical to unload on the Reader. The unload button latches down. The detent is removed and high bias pulls the tape back into the tape cartridge. The station cover unlocks when the tape is fully unloaded.

### LOAD

Load on the T.T.R. is similar to load on the MT/ST. The Operation Selector Switch must be in Record. When the load button is depressed, the tape loads to the Beginning of Tape slot. The tape is then stepped to the first recordable track where a Feed (1,3,5) code is recorded and the load operation is complete. The Feed code is supplied by the Logic, not the PRECON. Once the tape is loaded, the load key contact is inactive.

### RE-RECORD

The Re-record key contact is inactive unless the T.T.R. stops in an error condition. Automatic Re-record must be discussed before Re-record is explained.

If an error is detected on the Backstroke, the Logic in the T.T.R. automatically attempts to Re-record the code. If it succeeds, the operation continues. If it fails, the T.T.R. stops with the Error light on.

Re-record and Automatic Re-record are identical operations except for the way they are initiated.

In either case, the tape has stepped after the Error is detected. The Tape deck takes two (2) cycles. The first cycle, either automatic or from the Re-record button, records the code at this point and Backsteps the tape. (Recording the code in this track serves no purpose.)

On the second cycle the T.T.R. attempts to record the code in the track where the Error occurred and the tape steps. If the code records without Error the operation continues.

If the Error cannot be corrected, the problem may be a damaged tape or the End of Tape slot (see EOT light).

REMEMBER, any time the T.T.R. stops with the Error light on, it has already attempted to Re-record the code one time.

### OPERATION SELECTOR SWITCH

The Operation Selector Switch has two positions:

1. Record
2. EOT Release

Record is the normal position for this switch. It must be in the Record position to load or record a Third Tape. If a Third Tape is not desired, the C.C.U. Control Panel must be used to "turn off" the Recorder, NOT this switch.

The EOT Release position should ONLY be used to release the PRECON in case of an uncorrectable error condition.

This position of the switch does NOT turn the T.T.R. off. It completes a feedback loop which will release the PRECON. The T.T.R. still has power on and a Character Counter in the PRECON is active. This Character Counter is used to determine when the T.T.R. is near the end of a 100 foot Tape. Leaving the switch in this position falsely indicates to the PRECON that the Third Tape is being recorded.

In the event of an uncorrectable error, such as a damaged tape or inadvertently reaching the End of Tape Slot, the following procedure should be used:

1. If using the Re-record button cannot correct the error, mark the Output line that was being printed when the error occurred.

2. Depress Line Stop and then place the Operation Selector Switch in the EOT Release position. The printer will immediately resume printing.
3. When printing stops, mark the line the Carrier is on.
4. Unload the Third Tape and load another one.
5. Answer the Third Tape decision on the Control Panel with "New Tape" and resume operation. (This will record a Reference code and reset the Character Counter.)

*NOTE: The Text that played out with the switch in the EOT Release position is NOT on the tape. These lines including the one with the error, must be Merged in at the next updating of this project. The Hard copy produced when the error occurred is correct and can be used.*

*When preparing the Merge tape, consider these TWO tapes as ONE tape. The Merge tape should contain a Stop code to allow the first tape (containing the error) to be unloaded and the second tape loaded.*

## READY LIGHT

The Ready Light will glow when the Operation Selector Switch is in Record and the tape is loaded. Placing the switch in the EOT Release position will cause the Ready Light to go out. It will glow again if the switch is returned to Record. A power interruption to the T.T.R. will cause the Ready Light to go out. Restoring power WILL NOT cause the Ready Light to glow again. The Third Tape must be reloaded before the Ready Light will come back on. The Ready light indicates the T.T.R. is ready to accept Output Program Steps.

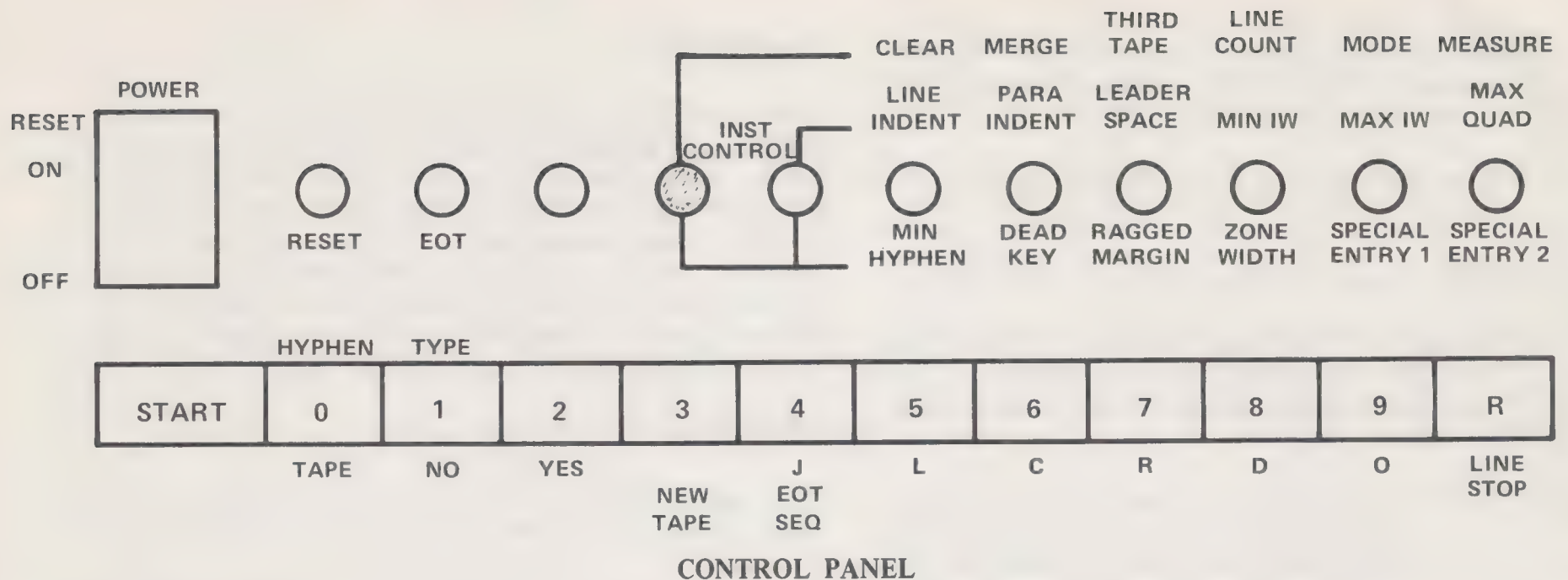
## EOT LIGHT

This Light indicates an error on tape that has not been corrected (possible damaged tape or End of Tape Slot).

Normally, the End of Tape Slot will not be reached because the PRECON counts the Characters and stops the operation before the end of a 100 foot tape is reached. This is discussed under the heading "End of Tape Sequence".

If a short tape is used or the Operator answers "New Tape" after partially recording a 100 foot tape, the End of Tape Slot may inadvertently be reached.

"New Tape" is a Control Panel decision that resets the Character Counter. It will be explained Later.



### CLEAR - Yes or NO

When the "Clear" decision is answered "Yes"

1. All Text in Memory is cleared.
2. Merge is set to NO.
3. Third Tape is set to NO.
4. Line Indent is set at Zero.
5. Line Count is restored to the last value entered.
6. Input Line Count is reset to zero.
7. Any Address Code Line Number, stored in Memory is cleared (Merge Address).
8. All other information remains unchanged.

When NO is entered or an entry is not made.

1. Text will remain in Memory.
2. All instructions previously entered will remain unchanged.

### MERGE - Yes or An Entry is NOT Required.

Answer YES if a Correction Tape is loaded.

*NOTE: In order for the MT/SC to respond properly to a YES Answer, the Clear Light MUST first be answered YES.*

Answering NO does NOT have any effect on the machine operation.

*NOTE: Remember, Merge is automatically reset to NO when the Clear Light has been answered YES. The Merge Decision will also be changed to NO if an Address Cancel Code (prefix-a-comma-CR) is read from the Left Tape.*

### THIRD TAPE - New Tape, Yes, No or EOT Seq.

The Control Panel decision of "Third Tape" has been added by this feature. It can be answered in one of four ways:

1. Answering Third Tape with New Tape causes the following to occur when Tape-Start is depressed:

- A. The Carrier spaces the amount of the stored measure, Tabs once and prints an upper case "X".

*NOTE: If NEW TAPE is NOT preceded by CLEAR-YES, the carrier will only space to the right edge of the measure before tabbing.*

- B. A Reference code is recorded on the Third Tape.
- C. A Character Count in the PRECON is reset to zero. This Character Count is used to determine when the T.T.R. is near the end of a 100 foot tape. This will be discussed further under the heading "End of Tape Sequence."

*NOTE: The Character Counter is reset when START is depressed to store the decision.*

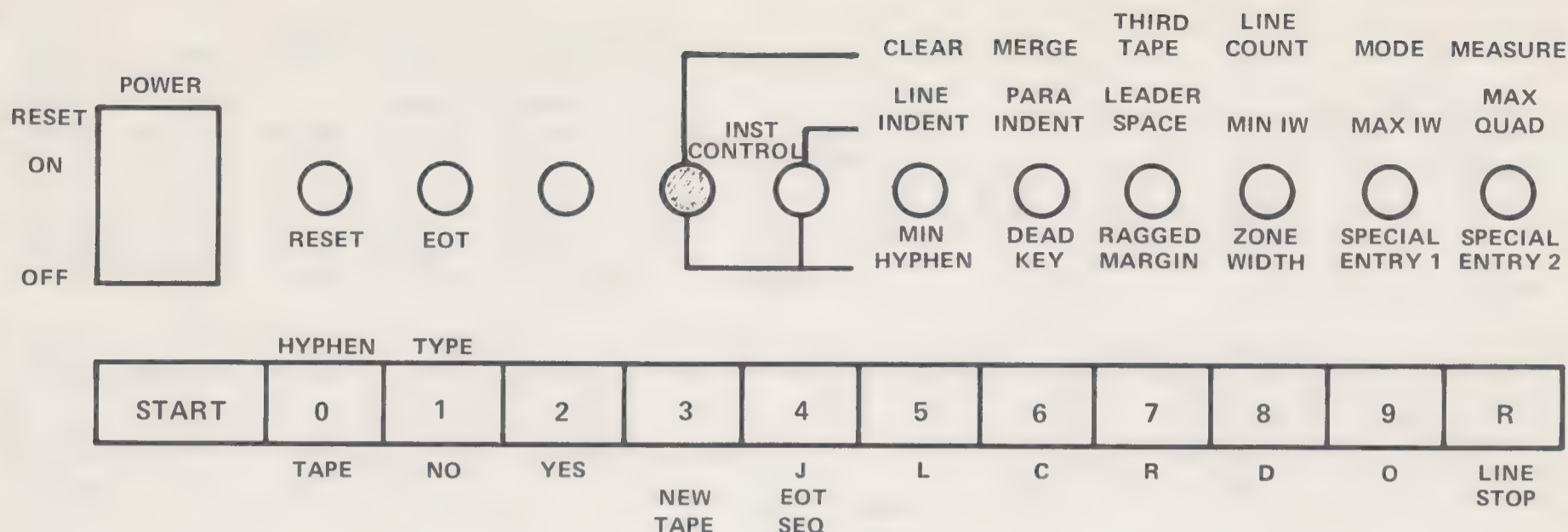
- D. The MT/SC will then stop with the Line Count Light on (see Line Count).

2. Answering Third Tape with YES will be necessary under the two following conditions:

- A. Answering CLEAR-YES changes Third Tape To NO.  
If Third Tape is Answered YES after CLEAR-YES, when TAPE-START is depressed Items 1-A,B&D above will occur. Item 1-C will not occur.

- B. Third Tape was changed to NO to omit one or more lines. To resume recording, Third Tape would be changed to YES. Changing the Third Tape decision for this purpose will NOT result in a Reference code being recorded as long as it isn't preceded by CLEAR-YES.

3. Answering Third Tape with NO results in no Output to the T.T.R. and stops the Character Counter. (Third Tape is Automatically set to NO when CLEAR is answered YES.)



**NOTE:** The use of these three different decisions will be more apparent after reading about recording Reference codes.

- Answering Third Tape with EOT Seq. will cause an End of Tape Sequence to be recorded on the Third Tape. Normally this is recorded automatically when the Character Counter detects that the tape is full. It can be entered manually if the MT/SC is to be turned OFF (overnight) before a project is completed. (A power interruption requires the tape to be reloaded.)  
For further information, see "End of Tape Sequence".

**LINE COUNT** - A Number between 1 and 32,000

Line Count is used to record a Reference code on the Third Tape.

When the entered number of Output lines has played out, the MT/SC will stop with the Line Count Light on. When this happens, one of the following will apply:

- IF A REFERENCE CODE IS DESIRED AT THIS POINT, depress TAPE-START. The printer spaces to the right edge of the Measure, Tabs once, prints an upper case "X", records a Reference code and stops with the Line Count Light on again. Line Count or any other Control Panel entries can be changed at this time. If all entries, including Line Count, are still valid, simply depress TAPE-START to resume operation.
- IF A REFERENCE CODE IS NOT DESIRED AT THIS POINT, enter a new Line Count. Any valid number may be entered, including the one previously used. Depress START to store the entry, then TAPE-START. Payout and Recording will resume without recording a Reference code.

**NOTE:** When the MT/SC stops with the Line Count Light on, the Carrier will be resting at the end of the last Output line.  
CLEAR-YES, THIRD TAPE-YES at this point will cause the Carrier to space the amount of

the Measure, Tab, print an "X" and record a Reference code. Although it is recommended that three Tab stops be set to the right of the measure, this "X" may print off the paper.  
**SOLUTION:** Do not use Line Count to play down to a point where CLEAR will be Answered YES.

**MODE** - Justify, Flush Left, Center, Flush Right, Dot Leader or Outline.

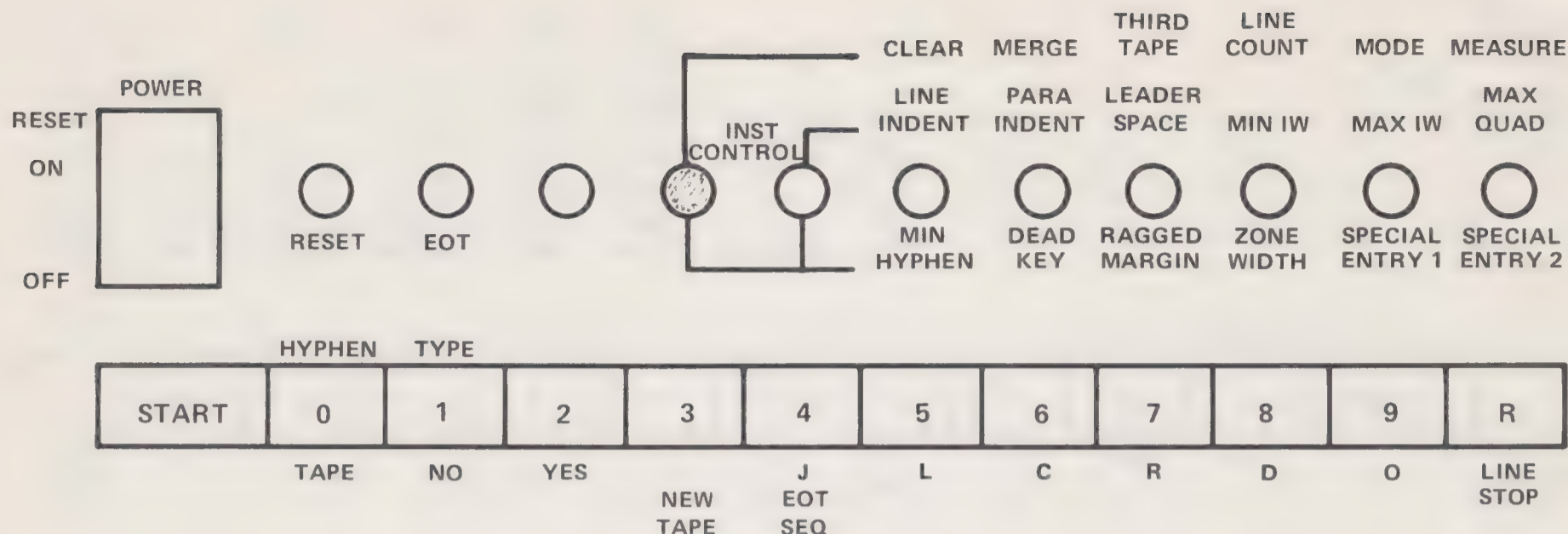
**MEASURE** - Maximum Measure = 940 units.

### SUMMARY OF MODE AND MEASURE

To understand how Mode and Measure relate to preparing a Third Tape the following information needs to be considered:

- Line endings on the Third Tape will match line endings on the original tape(s) in all non-justify Modes.
- The Measure controls the line endings on the Third Tape when in the Justify Modes. Line endings on the Third Tape will match line endings on the Output copy.
- All Graphics codes read from the Tape, except Address Information and Reference codes, will be recorded on the Third Tape. Decisions Keyed in at the Control Panel WILL NOT be recorded on the Third Tape.
- Dot Leaders are not recorded on the Third Tape, only the Code for Dot Leadering.
- Spaces preceding Flush Right, Centered or Indented Text are not recorded on the Third Tape.

The foregoing statements relate to Mode and Measure, either read from the tape or keyed in at the Control Panel. If the Mode and Measure are read from the tape, they will be recorded on the Third Tape. The Third tape



will match the Hard copy. Another identical Output Copy can be obtained by playing out the Third Tape. (IDENTICAL CONTROL PANEL DECISIONS MUST BE USED IF AN IDENTICAL OUTPUT COPY IS DESIRED.) If the Mode and/or Measure were keyed in at the Control Panel, they WILL NOT be recorded on the Third Tape.

**LINE INDENT** - no or from 2 to a value less than the Measure.

*NOTE: Line Indent MUST NOT be used when operating in the "Outline" Mode. Remember, "CLEAR-YES" resets Line Indent to zero.*

**PARAGRAPH INDENT** - NO or a value of 2 to 255 Units.

**LEADER SPACE** - A number between 3 and 255 Units.

**MINIMUM INTERWORD** - A number between 2 and 255 Units.

**MAXIMUM INTERWORD** - A number between 2 and 255 Units.

**MAXIMUM QUAD** - A number between 2 and 255 Units.

**MINIMUM HYPHENATION** - Yes or No.

1. Yes - MT/SC will resort to Interletter spacing before "asking" for Hyphenation (practically no Hyphenation decisions).
2. No - MT/SC will "ask" for a Hyphenation before resorting to Maximum Quad.

**DEAD KEY** - Yes or No

1. If YES is answered - Release Dead Key Disconnect and set the Velocity Control.
2. If NO is answered - Lock down the Dead Key Disconnect and set the Velocity Control.

**RAGGED MARGIN** - Yes or No

If Mode was answered either "J" or "O", an answer of YES will cause the copy to be played out with a ragged right margin. (Similar to adjust on the MT/ST.) The degree of raggedness and the actual line endings are determined by the answer keyed in for the Zone Light. When Ragged Margin is answered YES and the system is in "J" or "O" Mode, all spaces between words will be the Value entered for "Minimum Interword". All lines will end after the LAST word in the Zone that does NOT exceed the Measure.

If Mode was answered either "J" or "O" an answer of NO for Ragged Margin will cause the copy to be played out with the right margin Justified.

This entry has no effect on the other Modes.

*NOTE: The Ragged Margin Light does NOT come on with some PRECONs such as 2613.*

**ZONE** - A number between 2 and 255.

This entry creates a Zone from the end of the Measure back to the left for the PRECON to detect a place to break the line. If a place is not detected, the word that extends across the Zone will print out for hyphenation. If the hyphenation is rejected, that line will end short of the Zone and that word will print on the next line down. (All spaces are the value entered for "Minimum Interword".)

*NOTE: Increasing the Zone width will decrease hyphenation decisions. (50 units = Approximately 10 characters.)*

**SPECIAL ENTRY 1 & 2** - Not Presently Being Used.

## OPERATION OF THE T.T.R.

### OUTPUT TO THE T.T.R. PROGRAM STEP

The T.T.R. is Device code 4. The Program Step might be written: OT4,2. This means "Output" to "Device 4" from "Register 2".

The Program Step Set is as follows:

op1	op2	op3	op4	op5	op6	ADDRESS	op7
0	0	0	1	0	0	1 0 0 0	0

This Program Step works like any other Output P.S.

**NOTE:** When using a PRECON that can record a Third Tape, Multiplex Output is not used. If a Third Tape is not to be recorded, a change back to a Third Tape Related PRECON will speed up the thru-put. Tapes recorded on the T.T.R. CANNOT be played back with PRECONS 256, 260, 261 or 259.

### REFERENCE CODES

Recording a Reference code on the T.T.R. is a function of the PRECON. This function can be initiated three ways:

1. An answer of NEW TAPE to the Control Panel question THIRD TAPE will result in the recording of a Reference code when TAPE-START is depressed. This also resets a character count in the PRECON to zero. The Character Count is used to determine when the T.T.R. is near the end of a 100 foot tape. Because of the Character Count, NEW TAPE MUST only be used for the first Reference code on each tape.

When TAPE-START is depressed, the following will occur:

- A. The carrier will space to the Right edge of the Measure,

**NOTE:** If NEW TAPE is preceded by CLEAR-YES the carrier, regardless of its position, will space the amount of the entered Measure.

- B. Tab once,
- C. Print an upper case "X",
- D. Record a Reference code on the Third Tape,
- E. Reset the Character Count to zero.

2. Answering CLEAR-YES, THIRD TAPE-YES will result in recording a Reference code when TAPE-START is depressed. This does NOT reset the Character Count.

**NOTE:** THIRD TAPE-YES not preceded by CLEAR-YES will change the Third Tape decision to YES, but will NOT cause a Reference code to be recorded. Remember, CLEAR-YES changes THIRD TAPE to NO.

This procedure for recording a Reference code should be used any time it is necessary to answer

CLEAR-YES, such as between Projects. When TAPE-START is depressed, the following will occur:

- A. The Carrier, regardless of its position, will space the amount of the entered Measure,
- B. Tab once,
- C. Print an upper case "X",
- D. Record a Reference code on the T.T.R.

3. When the Output Line Count value is reached and the MT/SC stops with the Line Count Light on, a Reference code can be recorded by depressing TAPE-START. This procedure is to be used for recording Reference codes between pages. It does NOT reset the Character Count.

When TAPE-START is depressed, the following will occur:

- A. The Carrier will space to the right edge of the Measure,

**NOTE:** Remember, when the MT/SC stops with the Line Count Light on, the carrier will be resting at the right end of that line. If the line fills the Measure, no spacing will occur.

- B. Tab once,
- C. Print an upper case "X",
- D. Record a Reference code on the T.T.R.

**NOTE:** If No Reference code is desired when the MT/SC stops with the Line Count Light on, a number MUST be entered. Any valid number may be entered, including the one previously used.

In all three procedures, after the T.T.R. has recorded the Reference code, the MT/SC will then stop with the Control Panel Line Count Light glowing and the carrier to the right. This gives the operator an opportunity to change the Line Count value. This is necessary because of the relationship between Line Count and Reference codes.

### HYPHENATIONS

Hyphenation decisions made at the Control Panel will effect both the Output copy and the Third Tape being recorded.

The following should be understood:

1. The MT/SC attempts to Justify (or Ragged Right) each line, without violating the entries made at the Control Panel (Max IW, Max Quad & Min Hyphenation).
2. If it cannot do this, it prints out a word for hyphenation.
3. In some cases a Hyphenation decision can be made that will still force the MT/SC to violate the Control Panel entries. (Bracket far to the right; Hyphen entered far to the left.)
4. If the Hyphenation decision is refused, the MT/SC will always have to violate the Control Panel entries.

Basically there are two types of Hyphens:

1. Required Hyphen - "Mother-in-law".
2. Syllable Hyphen - Use of a Hyphen between syllables of a word that would not require one if the word were printed on one line.

When a Syllable Hyphen decision is made:

1. A Space, Backspace, Hyphen, CR code records on the Third Tape.
2. This word will be hyphenated at this point automatically on later playback of this Third Tape, providing;
  - A. The same Control Panel entries are used.
  - B. This decision, when made, didn't cause the MT/SC to violate the Control Panel Entries.
3. This word may be joined together without the Hyphen if on later playback of this tape, different Control Panel decisions (including Measure) are used.

*NOTE: If another Third Tape is being prepared in Item 3, the Sp, BS, Hyphen will still be recorded on the new Third Tape. Also, if this word is hyphenated in a different place, both Sp, BS, Hyphen codes will be recorded on the new Third Tape.*

When a word is divided at a Required Hyphen:

1. A Hyphen, Space, Backspace, CR code records on the Third Tape
2. This word will NEVER be automatically divided on later playback of this tape.
3. If this word is NOT Manually Hyphenated at this point when using this tape to generate a new Third Tape, the Sp, BS code WILL NOT be recorded on the new Third Tape.

## END OF TAPE SEQUENCE

To prevent recording beyond a 100 foot tape's capacity, the T.T.R. PRECON counts characters (all codes) as they are sent to the T.T.R. When approximately 21,500 codes have been recorded, the MT/SC does the following:

1. The system (including the T.T.R.) completes the line it is working on.
2. The carrier tabs to the right and prints an uppercase "E".
3. The T.T.R. records an End of Tape Sequence which consists of one CR code; a 3,4,7 code (redundant) and two Stop Transfer codes (all these codes are supplied by the PRECON).
4. The RED "Instruction Control" light and the Third

Tape light comes ON on the Control Panel and the system stops.

This indicates a full tape. The tape should be unloaded, another tape loaded and the Control Panel decision answered NEW TAPE. The Character Count is reset to zero. TAPE-START will cause a Reference code to be recorded on the new Third Tape and the operation can be resumed.

When read by the Reader, this End of Tape Sequence will cause the C.C.U. to stop with the Clear light and the Merge light on. The last line from the tape has not printed out at this time, but is stored in Memory. Although the MT/SC is stopped, no Control Panel entries can be made. The tape should be unloaded and the tape containing the continuation of the text loaded. Depressing START will cause the operation to resume.

The information from the two tapes will join together as though it was all recorded on one tape. This will be true even if it occurs in a Justified paragraph. Remember that the End of Tape Sequence should only occur at the end of a recorded line.

The End of Tape Sequence can also be entered at the Control Panel when the Third Tape Light is on. This should be done if the MT/SC is to be turned OFF for any reason before the project is completed.

The foregoing information relative to Recording and Playing back the End of Tape Sequence applies, regardless of how it was generated (Character Counter or Control Panel).

## HEAD ALIGNMENT

Three lights are used for head alignment.

1. The READY light will indicate a ONE bit for Along the Tape or a FOUR bit for Across the Tape.
2. The ERROR light will indicate an EIGHT bit for Along the Tape or a FIVE bit for Across the Tape.
3. The "C" light (beside the C.E. Aid switch) will indicate a bit in the CENTER channel for Across the Tape.

Positioning the C.E. Aid switch to the right (toward the "C" light) will "free run" the Cycle Clutch and "no-step" the tape.

The alignment tolerances for the MT/ST, MT/SR and Reader apply to the T.T.R.

Initial alignment should be set up ALONG THE TAPE for a continuous READY and ERROR light (or NO lights if rocking sprocket slightly one direction turns on the READY light and rocking the opposite direction turns on the ERROR light).

Initial alignment for ACROSS THE TAPE should be set for a continuous "C" light with the READY and ERROR lights off.

When adjusting ACROSS THE TAPE, if the READY light (4 bit) glows, move the Head AWAY from the sprocket holes. If the ERROR light (5 bit) glows, move the Head TOWARD the sprocket holes.

### THIRD TAPE RECORDER LOAD

1. Depress Rec Load Keybutton
2. Rec Load sets  
*NOTE: Load Demand will be up because of Rec Common Res from unload or MR*
3. -Rec Ld↓ = can't get Rec Command SS until -Rec Ld↑
4. Load Search Shaft moves
5. Ld Sch Sol A = Detent removed & sch shoe on spring clutch
6. Tape goes into BOT slot
7. BOT Sw transfers = drop detent & Ld sch shaft restores
8. BOT Sw = BOT↑ = FD SETS & continuous pick to Rec Cy Cl  
*NOTE: CB 8 of first cycle = W/E Gate↑ = Ld Demand resets*
9. Step out of BOT slot
10. FORESTROKE (a cycle after BOT slot but before Oxide)
  - a. CB 8 makes & FD = W/E Gate↑
  - b. MP 1 = Beg Stroke↑ = C1↓ & C2↑  
*NOTE: Stepping of C1 & C2 on forestroke of Load serves no purpose.*
  - c. MP 3, 5, 8 & FD = Wr Nrml↑ = Write↑ = Try to write FD code
  - d. CB 8 breaks = W/E Gate↓
11. BACKSTROKE (a cycle after BOT slot but before Oxide)
  - a. MP 1 = Backstroke sets = Fore Step Mag picks
  - b. MP 1 also = Beg Stroke↑ = C1↓ & C2↑
  - c. No Bits read on backstroke = C1 & C2 don't change  
*NOTE: Error Latch is NOT used during Load.*
  - d. Step tape
  - e. Rec Home & FD = repick Rec Cy Cl
  - f. Rec Home also = Backstroke resets
12. FORESTROKE (cycle on first Oxide track)
  - a. CB 8 makes & FD = W/E Gate↑ = erasing tape
  - b. MP 1 = Beg Stroke↑ = C1↓ & C2↑
  - c. MP 3 & FD = Wr Nrml↑ = Write↑ = write a 1 Bit
  - d. MP 5 & FD = Wr Nrml↑ = Write↑ = write a 3 Bit
  - e. MP 8 & FD = Wr Nrml↑ = Write↑ = write a 5 Bit
  - f. CB 8 breaks = W/E Gate↓
13. BACKSTROKE (cycle on first Oxide track)
  - a. MP 1 = Backstroke sets = Forestep Mag picks
  - b. MP 1 also = Beg Stroke↑ = C1↓ & C2↑
  - c. Read Coil senses 5 Bit = Rec SA = BLE↑ (Bit Leading Edge)
  - d. BLE = C1↑
  - e. Rec SA then = BTE↑ (Bit Trailing Edge)
  - f. BTE = C2↓
  - g. 3 Bit sensed = Rec SA↑ = BLE↑ = C1↓
  - h. Rec SA then = BTE↑ = C2↑
  - i. 1 Bit sensed = Rec SA↑ = BLE↑ = C1↑
  - j. Rec SA then = BTE↑ = C2↓
  - k. MP 11 & C1 = Rec Ld resets (Rec Comm SS could come up)
  - l. Tape steps
  - m. -Rec Ld & Rec Home = Upset FD↑ = FD resets
  - n. Rec Home = Backstroke resets
  - o. Rec Cy Cl does not repick because FD is down.

### T.T.R. RECORD

The decision as to what code is sent to the T.T.R. is a function of the PRECON. The only decision made by the Logic in the T.T.R. relates to adding a Check (7) Bit if the code in the Recorder Output Latches is "even".

Assume recording of an "e", MT/ST 2,5,7 Bits = MT/SC Output Latches 2 & 3.

1. I-2 of an Output to Device 4 P.S. = Select Output Dev↑ = Recorder Sel sets
2. During I-5, B1-4 & B5-8 = Reset Output Latches & Ld Output Latches
3. I-5, B13-16 = Bsy↑ = Bsy\*↑ & Rdy↓
4. Bsy\* = Rec Comm SS↑ for 800 Micro Sec
5. Rec Comm SS & Bsy\* = reset Rec Output Latches
6. Rec Comm SS after 25 Micro Sec = Rec Comm SS Dly↑ = T.T. Interface Feedback↑ & Rec sets
7. TTIF = OIF\*↑ = BSY↓ = Bsy\*↓ = Res R.O.L.↓ = can load R.O.L. (2&3=e) from Output Latches (2&3)
8. Record & Rec Home = Rec Cy Cl picks
9. After 800 Micro Sec, Rec Comm SS↓ = (25 Micro Sec later) Rec Comm SS Dly↓ = TTIF↓
10. -TTIF = OIF\*↓ = Rdy↑
11. FORESTROKE
  - a. CB 8 makes & Rec = W/E Gate↑ = erasing tape
  - b. MP 1 = Beg Stroke↑ = C1↓ & C2↑  
*NOTE: Each MP will develop a Leading Edge (LE) & Trailing Edge (TE) signal*
  - c. MP 4 & R.O. 2 & Rec = Wr Nrml↑
  - d. Wr Nrml & LE & CB 8 = C1↑
  - e. Wr Nrml = Write↑ & W/E Gate = write a 2 Bit
  - f. TE & CB 8 = C2↓
  - g. MP 8 & R.O. 3 & Rec = Wr Nrml↑
  - h. Wr Nrml & LE & CB 8 = C1↓
  - i. Wr Nrml = Write↑ & W/E Gate = Write a 5 Bit
  - j. TE & CB 8 = C2↑
  - k. -C1 & -R.O. 7 & MP 10 & Rec = Wr 8 A/O 7↑
  - l. Wr 8 A/O 7 = Write↑ & W/E Gate = write a 7 Bit
  - m. CB 8 breaks = W/E Gate↓
12. BACKSTROKE
  - a. MP 1 = Backstroke sets = Forestep Mag picks
  - b. MP 1 also = Beg Stroke↑ = C1↓ & C2↑
  - c. If another Output to Device 4 P.S. is attempted before MP 1 time = Erly Pk sets = Rec Cy Cl repicks  
*NOTE: If Item 12-c is true, the Output Latches have changed, but the Recorder Output Latches have NOT.*
  - d. Read Head senses 7 Bit = Rec SA↑ = BLE↑ = C1↑  
*NOTE: Each Bit sensed will develop a Bit Leading Edge (BLE) & a Bit Trailing Edge (BTE)*
  - e. Rec SA then = BTE↑ = C2↓
  - f. 5 Bit sensed = Rec SA↑ = BLE↑ = C1↓
  - g. Rec SA then = BTE↑ = C2↑
  - h. 2 Bit sensed = Rec SA↑ = BLE↑ = C1↑
  - i. Rec SA then = BTE↑ = C2↓
  - j. MP 11 time  
*NOTE: The tape will step because of item 12-a. C1 up at MP 11 time means an "odd" code.  
MP 11 = MP 11 Dly↑ = Record resets.  
C1 down at MP 11 time means an "even" code (error).  
MP 11 & -C1 = Error sets = -E+B↓ = Record can't reset*
  - k. Rec Home = Backstroke resets

*NOTE: If Error is set, see AUTOMATIC RE-RECORD CHART.*

## AUTOMATIC RE-RECORD

If Early Pick was set by an Output to Device 4 P.S. the Recorder Cy Cl was repicked at MP 1 time on the Backstroke. If C1 is down at MP 11 time (on the backstroke) Error will set. As long as Error is UP, there will be a continuous pick on the Recorder Cy Cl. If both conditions above exist, the next code to be recorded is in the Output Latches, but the code that resulted in error is in the Recorder Output Latches. The tape will forestep. The Record Latch cannot reset because -E+B is down.

### END OF A RECORDER CYCLE WITH AN ERROR:

- A. Tape is one step beyond the error.
- B. The code is still in the Recorder Output Latches.
- C. Error is set, Record is still set & the Rec Cy Cl is repicked.

*NOTE: The Re-record Latch is not used for Automatic Re-record.*

1. FORESTROKE (First cycle after error)
    - a. CB 8 makes & Rec = W/E Gate↑ = erasing tape
    - b. MP 1 = Beg Stroke↑ = C1↓ & C2↑
    - c. MP 3 Thru MP 11 = record code one track too far down on tape

*NOTE: Item 1-c is immaterial, but it happens.*

  - d. CB 8 breaks = W/E Gate↓
2. BACKSTROKE (First cycle after error)
  - a. MP 1 = Backstroke↑ & Backstep↑ = Bstp Mag Log↑
  - b. MP 1 also = Beg Stroke↑ = C1↓ & C2↑ (not used but it happens)
  - c. Backstep tape to error track
  - d. Rec Home = Backstroke resets
3. FORESTROKE (2nd cycle after error)
  - a. CB 8 makes & Rec = W/E Gate↑ = erasing tape
  - b. MP 1 = Beg Stroke↑ = C1↓ & C2↑
  - c. MP 3 thru MP 11 = re-record code over error
  - d. MP 11 = MP 11 Dly↑ = Error resets = pick to Rec Cy Cl removed
  - e. CB 8 breaks = W/E Gate↓
4. BACKSTROKE (2nd cycle after error)
  - a. MP 1 = Backstroke sets = Forstp Mag Log↑ because -E B↑
  - b. MP 1 also = Beg Stroke↑ = C1↓ & C2↑
  - c. MP 11 time, if C1↑ = Bstp resets

*NOTE: If C1 is down = Bstp stays set (this is an error condition)*

- d. MP 11 = MP 11 Dly↑ & -E+B (if Bstp is down) = Rec resets
- e. Forestep the tape
- f. Rec Home = Backstroke resets
5. END OF AUTOMATIC RE-RECORD

If the code was recorded without a parity error (C1 up at MP 11 time) the next cycle will be a normal record cycle. If the code was recorded WITH a parity error (C1 down at MP 11 time) the cycle ends with: Error↓, Bstp↑, -E+B↓ & Rec↑

Bstp↑ = Error light on

Another Recorder cycle cannot be accomplished except by the Re-record Key or by unloading and reloading the tape.

## MANUAL RE-RECORD

A Manual Re-record cycle cannot be accomplished unless the Backstep Latch is set. The Backstep Latch being set indicates an error that Automatic Re-record couldn't correct. The code will still be in the Recorder Output Latches. The tape has stepped and the Record Latch is still set.

1. Depress the Re-record Keybutton
  2. Re-record Latch sets
  3. Release the Re-record Keybutton
  4. Error Latch sets = Rec Cy Cl picks
- NOTE: Rec Cy Cl remains picked until Error resets.*
5. FORESTROKE (1st cycle)
  - a. CB 8 makes & Rec = W/E Gate↑ = erasing tape
  - b. MP 1 = Beg Stroke↑ = C1↓ & C2↑
  - c. MP 1 also = Bstp resets
  - d. MP 2 = Re-record Latch resets
  - e. MP 3 thru MP 11 = record the code one step too far down on the tape

*NOTE: Item 1-e is immaterial, but it happens*

- f. CB 8 breaks = W/E Gate↓
- 6. BACKSTROKE (1st cycle)
  - a. MP 1 = Backstroke sets
  - b. MP 1 also = Beg Stroke↑ = C1↓ & C2↑ (not used but it happens)
  - c. MP 1 also = Bstp sets = Bstp Mag Log↑
  - d. Backstep tape to error track
  - e. Rec Home = Backstroke resets
- 7. FORESTROKE (2nd cycle after error)
  - a. CB 8 makes & Rec = W/E Gate↑ = erasing tape
  - b. MP 1 = Beg Stroke↑ = C1↓ & C2↑
  - c. MP 3 thru MP 11 = re-record code over error
  - d. MP 11 = MP 11 Dly↑ = Error resets = pick to Rec Cy Cl removed
  - e. CB 8 breaks = W/E Gate↓
- 8. BACKSTROKE (2nd cycle after error)
  - a. MP 1 = Backstroke sets = Forstp Mag Log↑ because -E B↑
  - b. MP 1 also = Beg Stroke↑ = C1↓ & C2↑
  - c. MP 11 time, if C1 is up = Bstp resets

*NOTE: If C1 is down = Bstp stays set (this is an error condition)*

- d. MP 11 = MP 11 Dly↑ & -E+B (if Bstp is down) = Rec resets
- e. Forestep the tape
- f. Rec Home = Backstroke resets.
- 9. END OF MANUAL RE-RECORD

If the code was recorded without a parity error (C1 up at MP 11 time) the next cycle will be a normal record cycle.

If the code was recorded WITH a parity error (C1 down at MP 11 time) the cycle ends with: Error↓, Bstp↑, -E+B↓ & Rec↑.

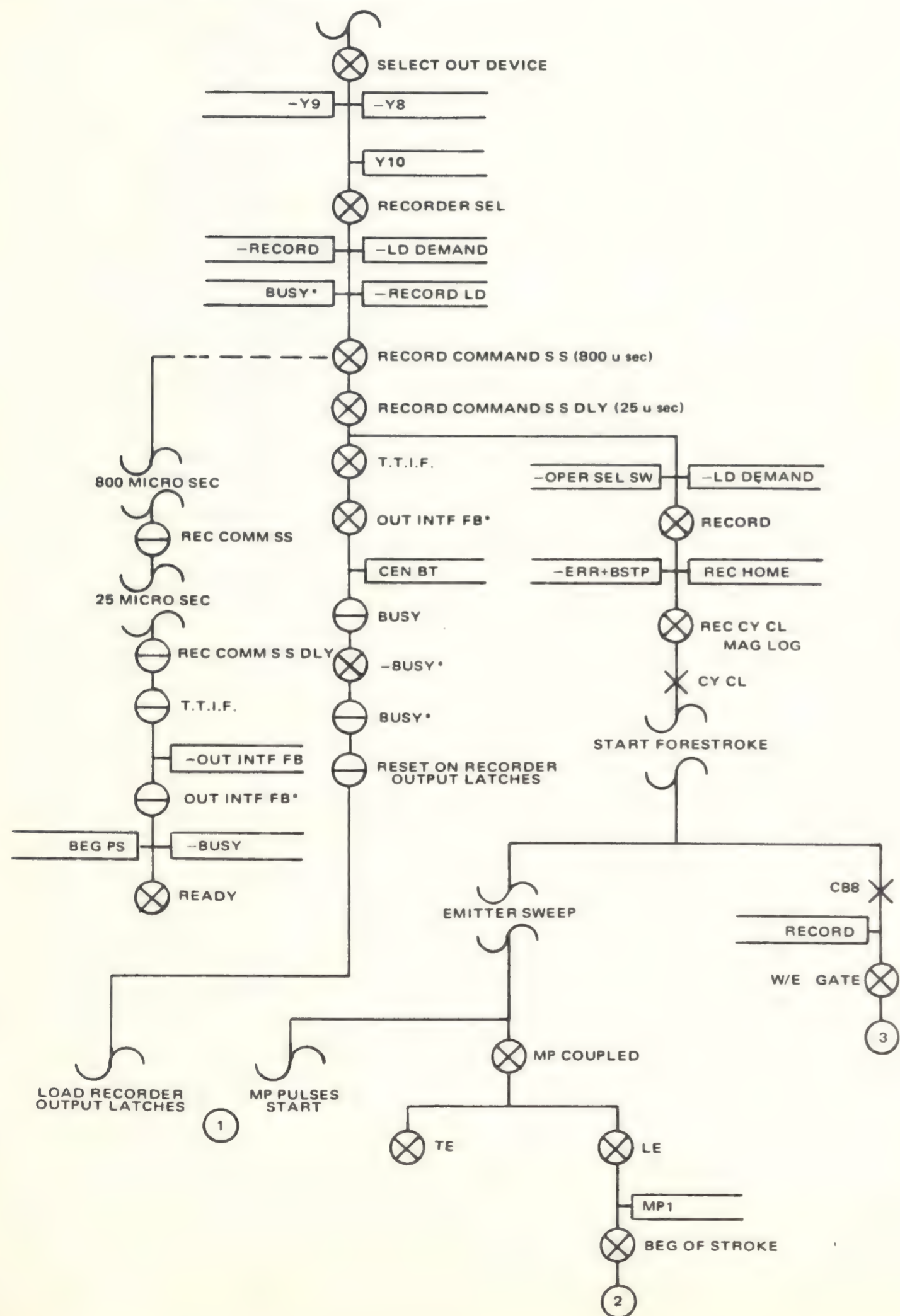
Bstp = Error light on.

Another Recorder cycle cannot be accomplished except by the Re-record key or by unloading and reloading the tape.

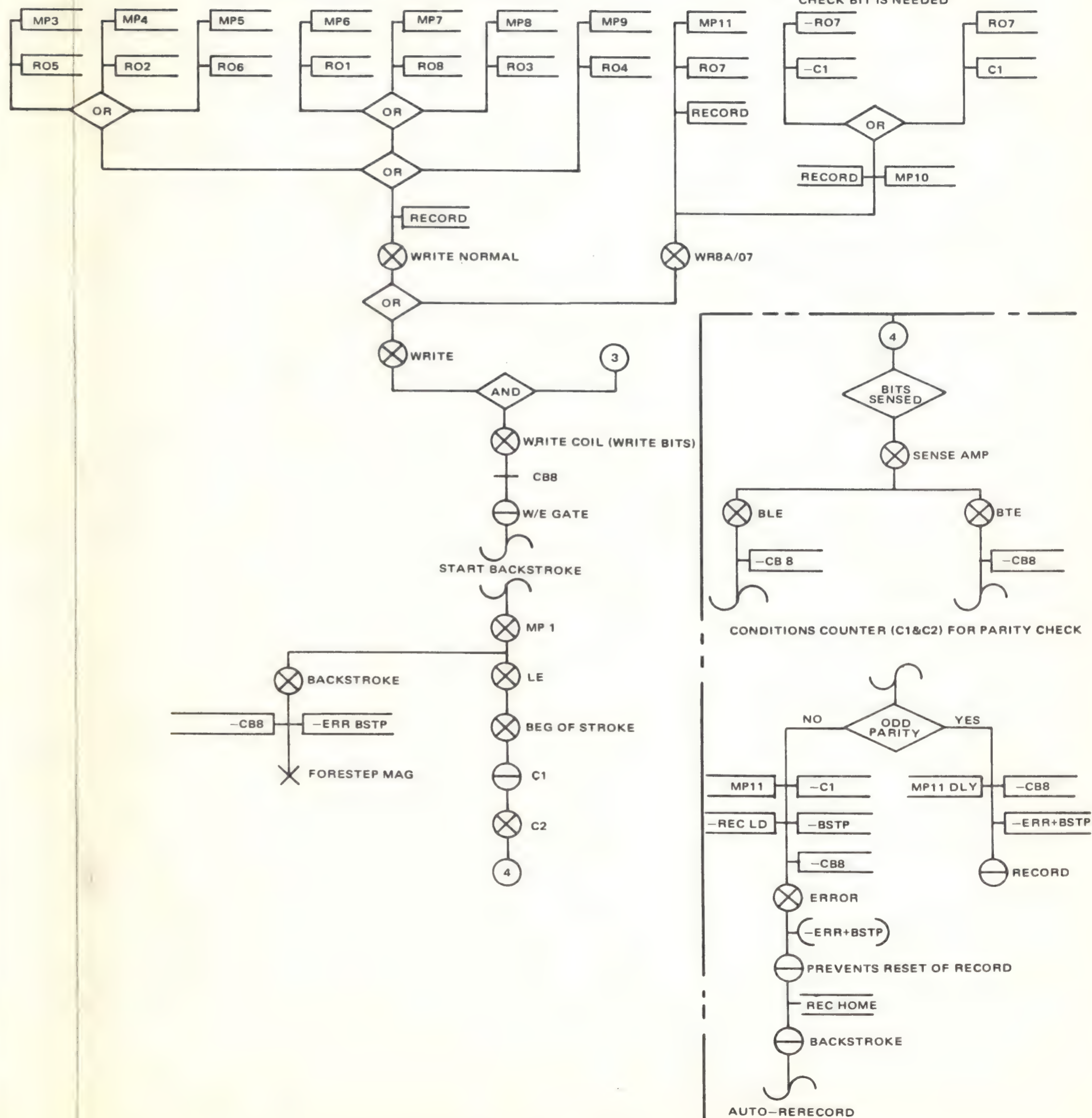


# RECORD

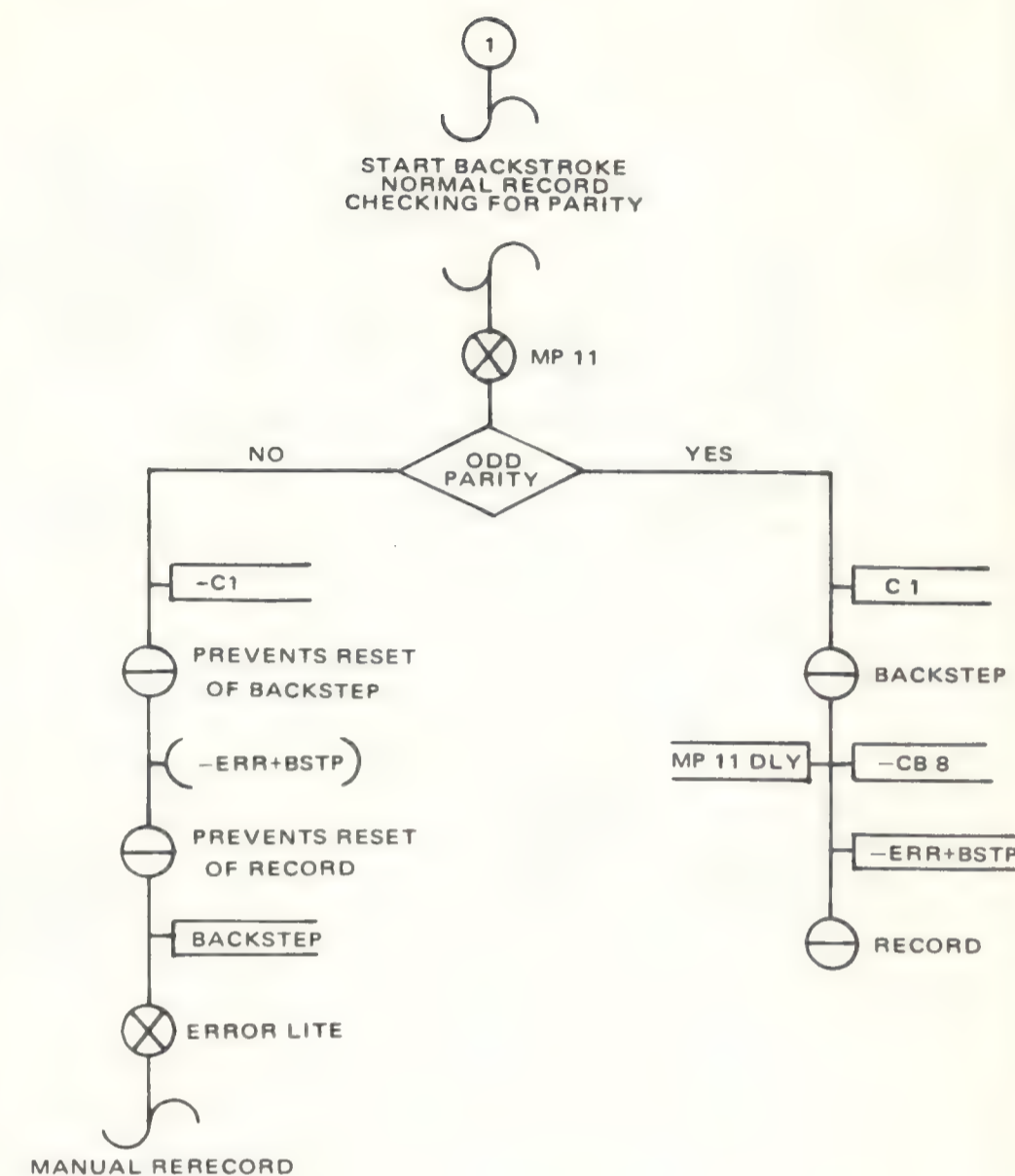
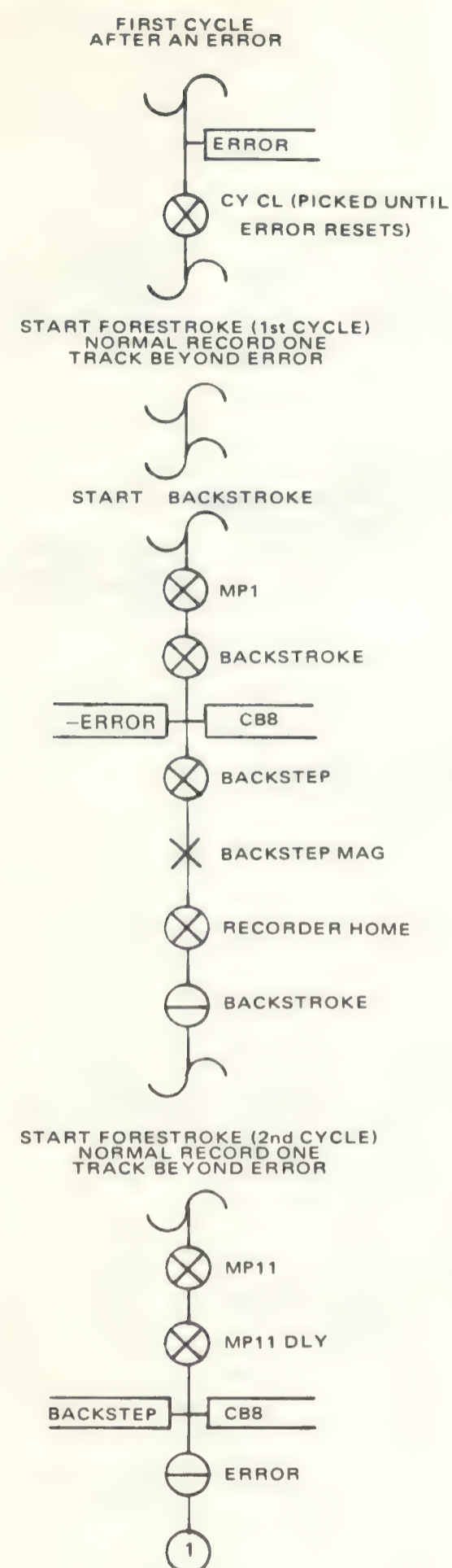
OUTPUT TO RECORDER P.S. (DEVICE CODE 4)



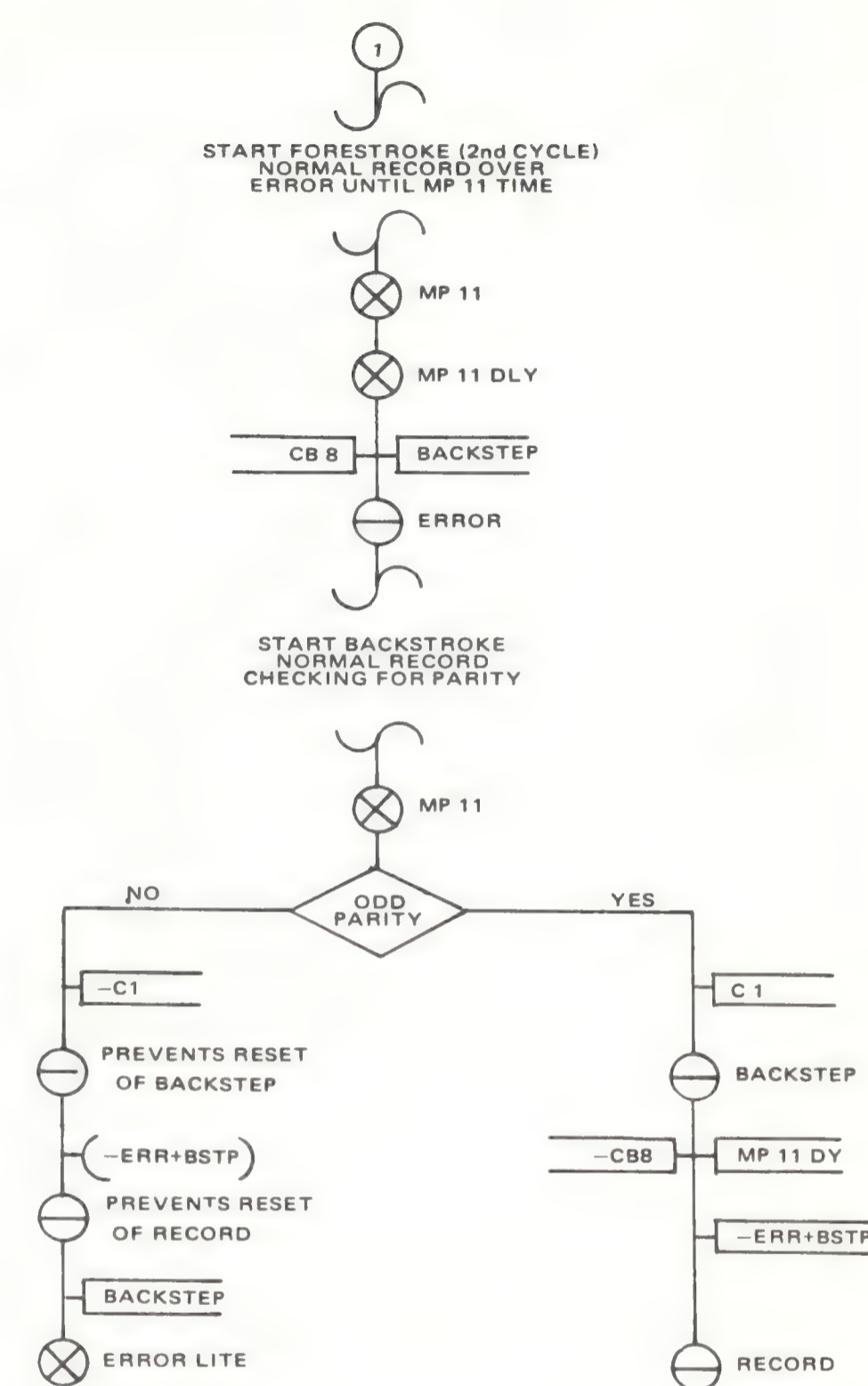
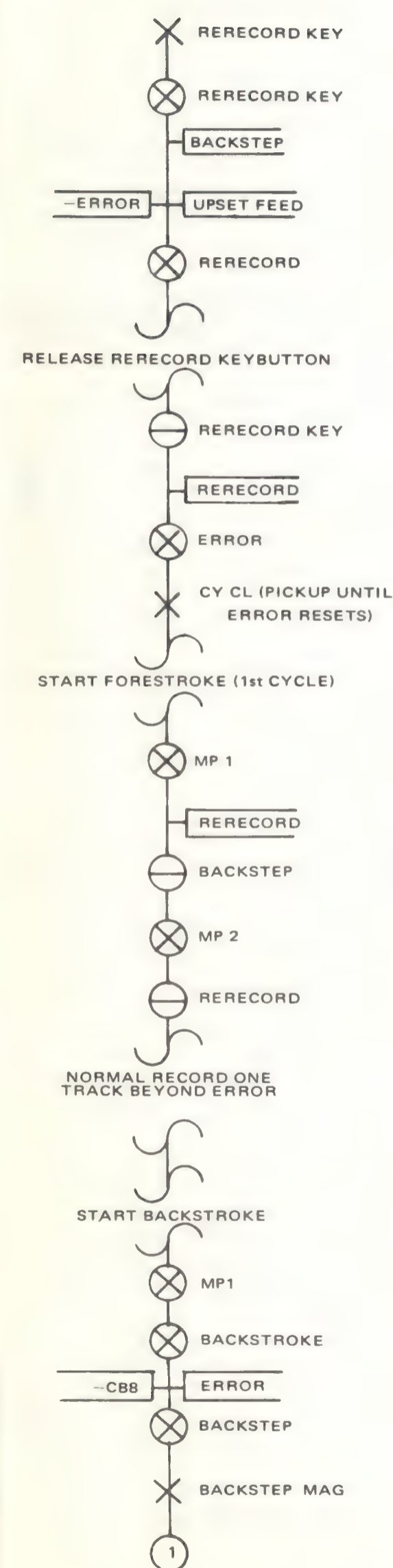
RECORD AS FOLLOWS DURING MP3 THROUGH MP11



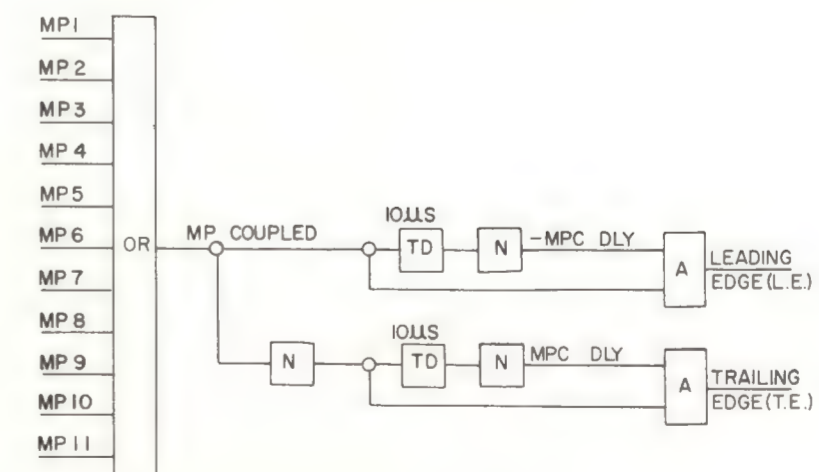
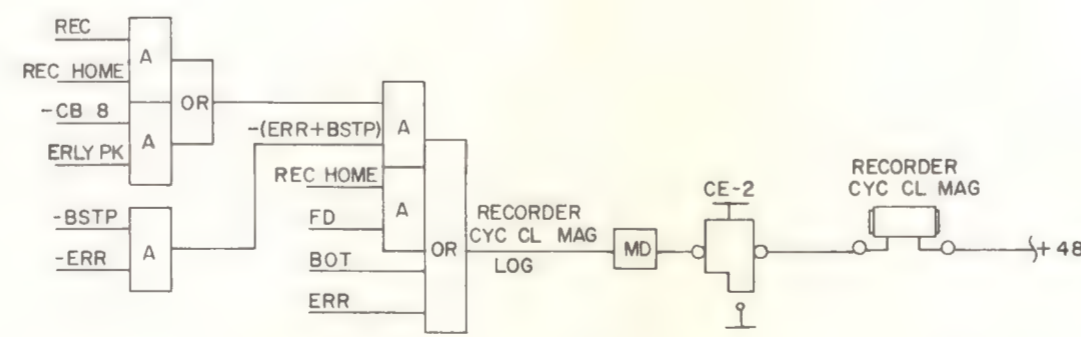
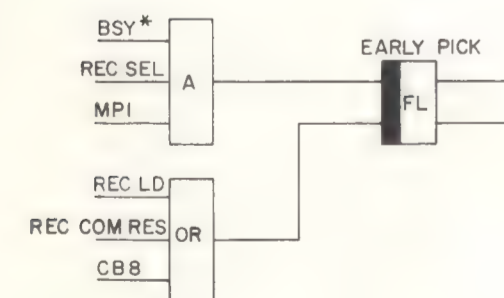
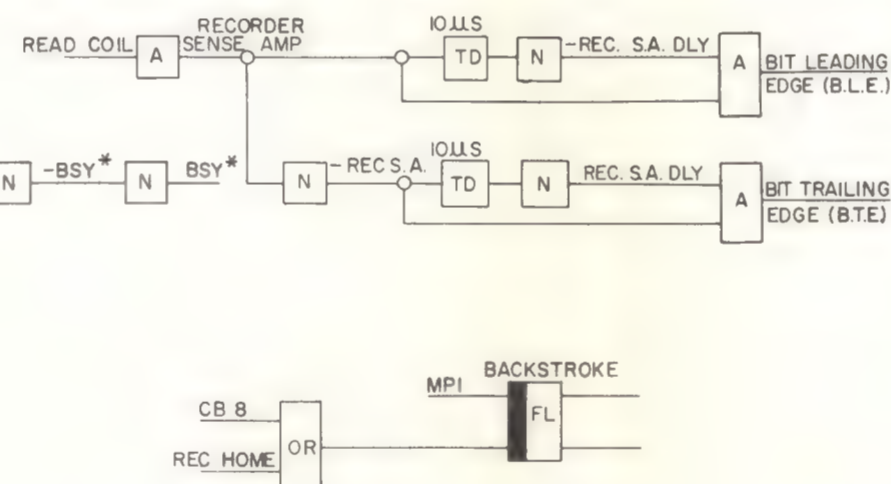
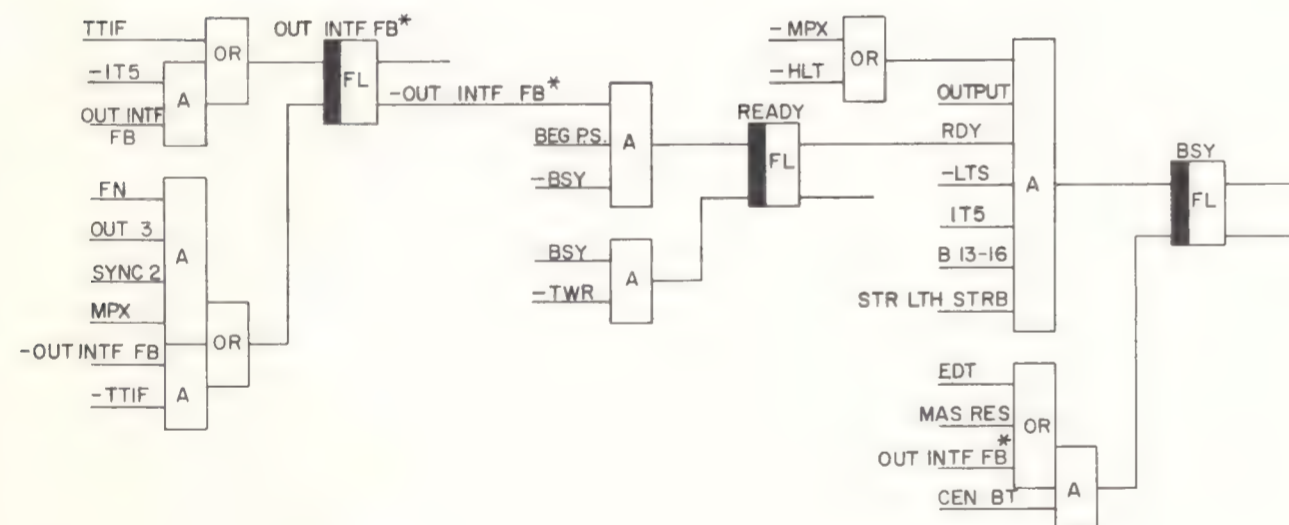
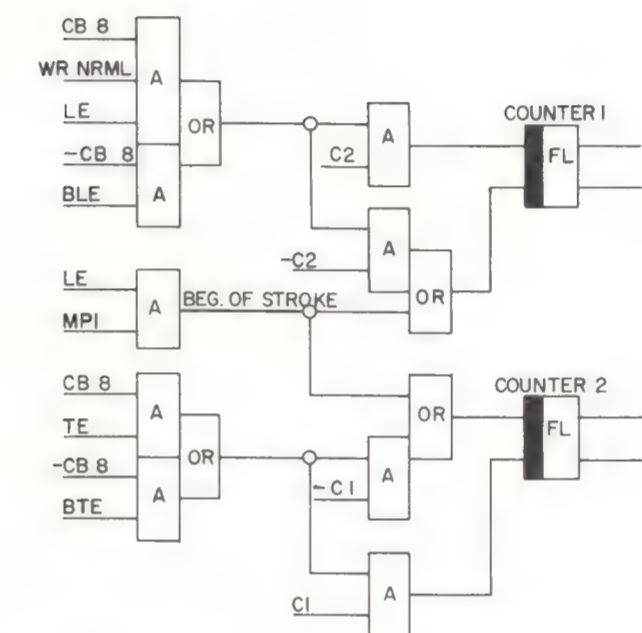
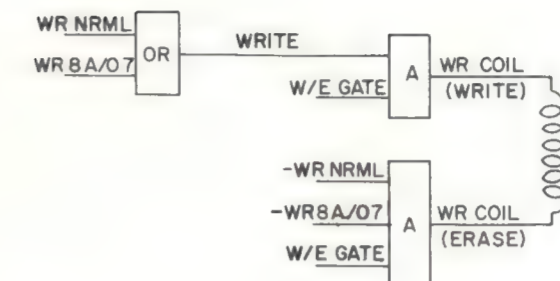
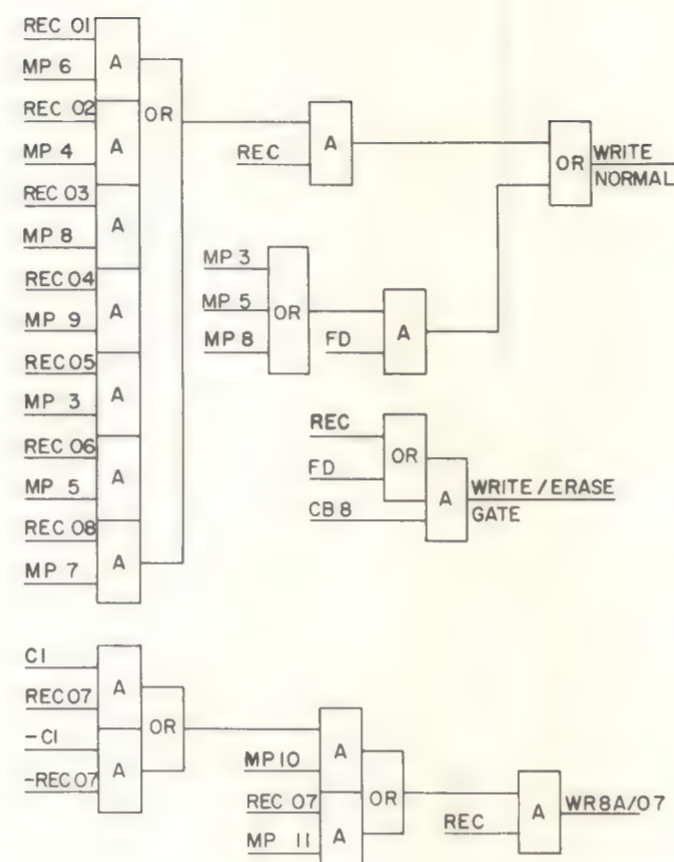
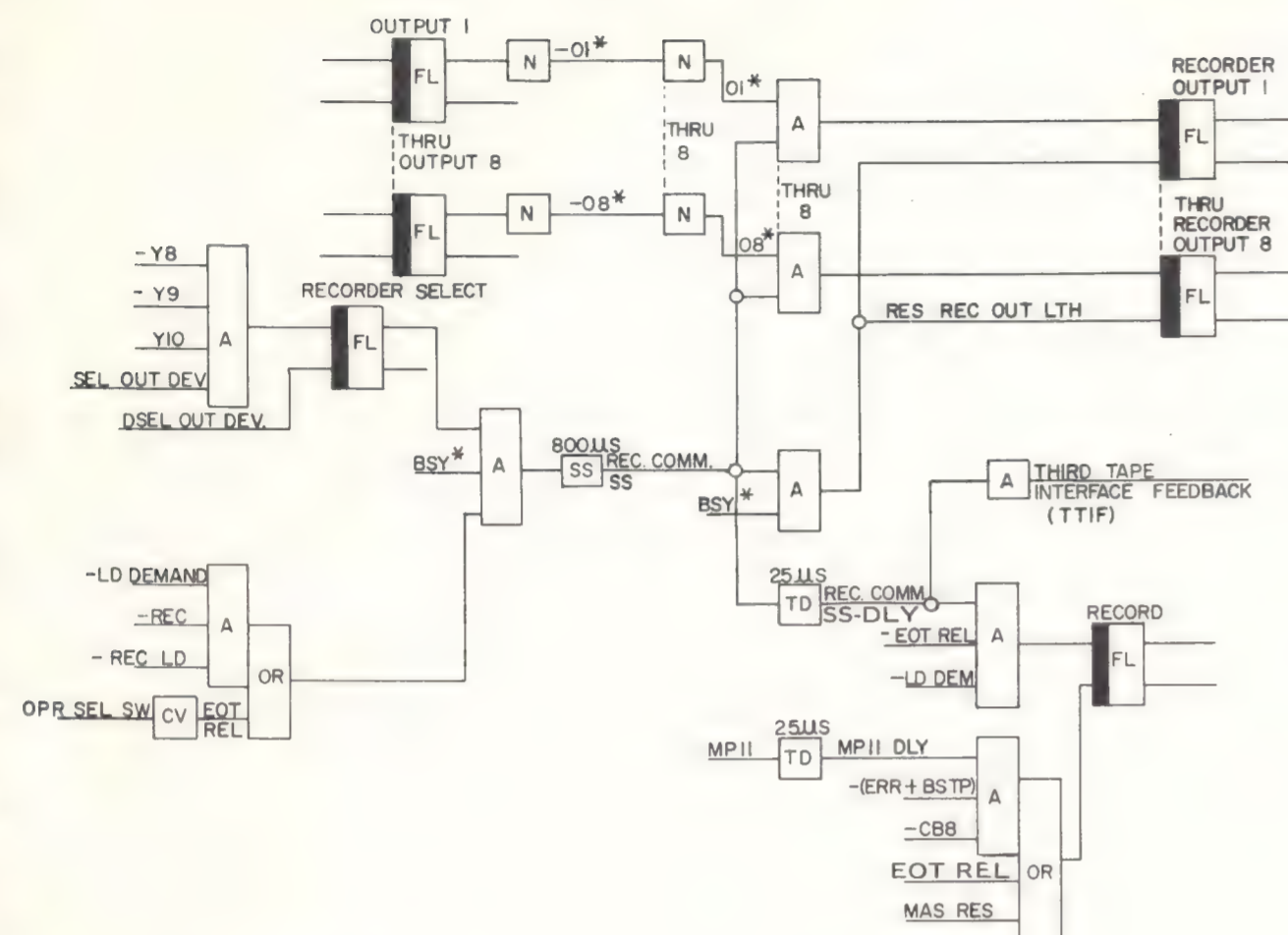
# AUTOMATIC RERECORD



# MANUAL RERECORD







DATE	E.C. NO.	DATE	E.C. NO.	OUTPUT LATCHES, CTRS, CTRL AND WRITE LOGIC	
20 MAY 69	580261A			PART NO. 1450384	PAGE NO. 0202
				IBM 6340	





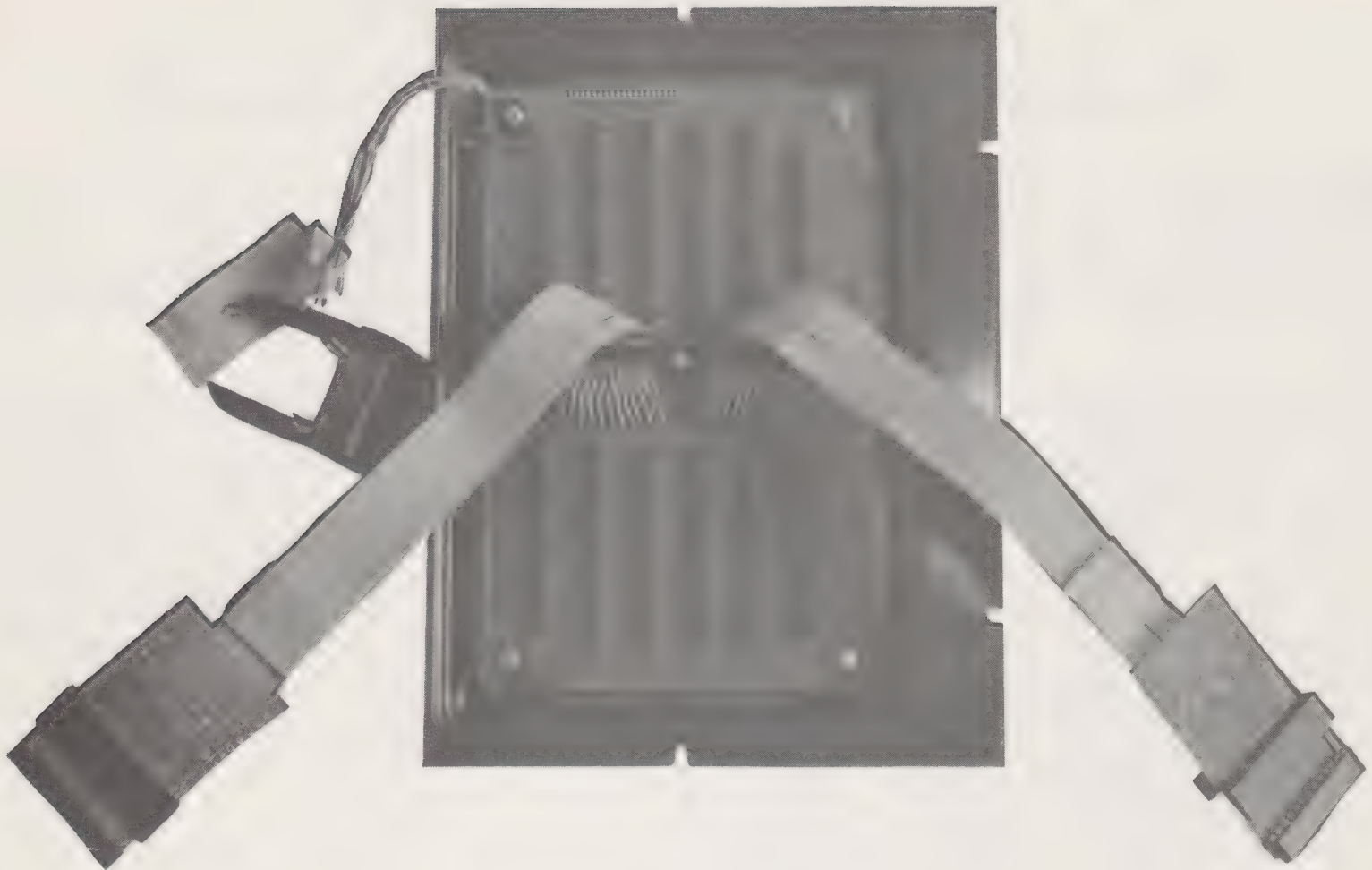
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(Alphabetical)

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NEW 23K MEMORY



PRESENT 16K MEMORY

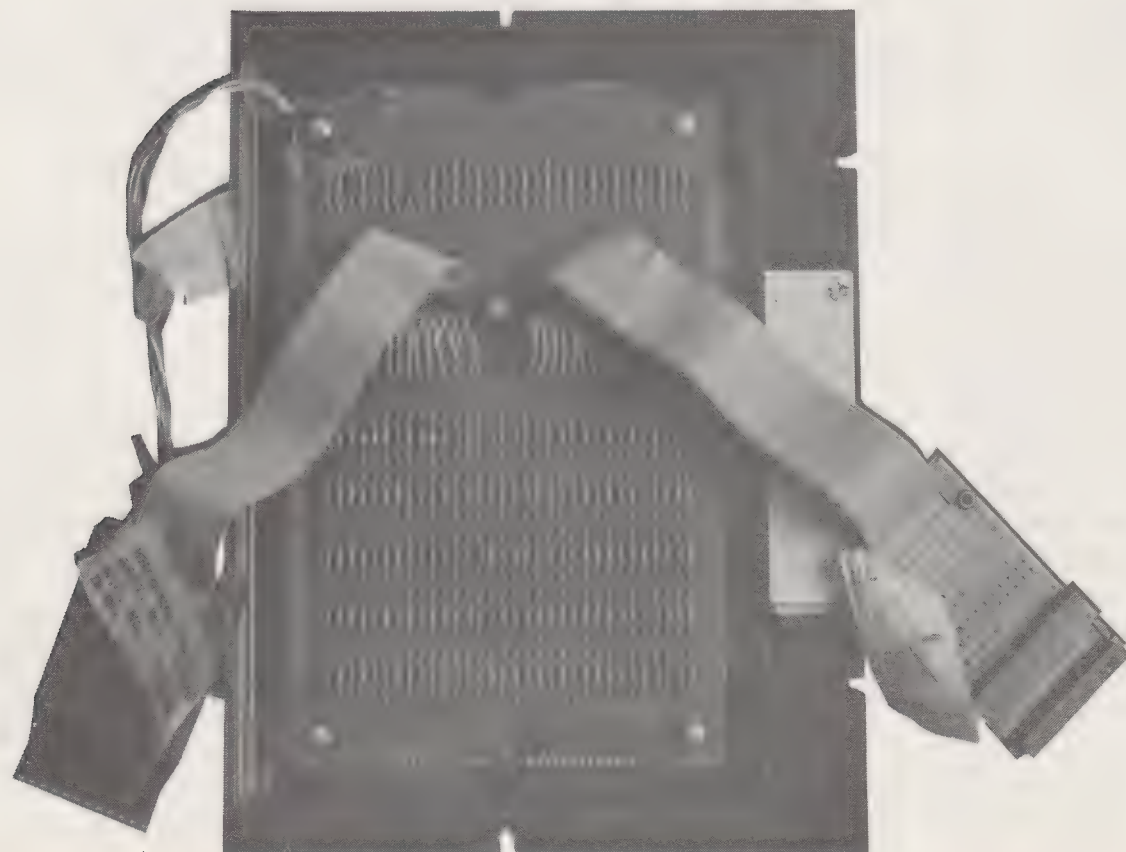
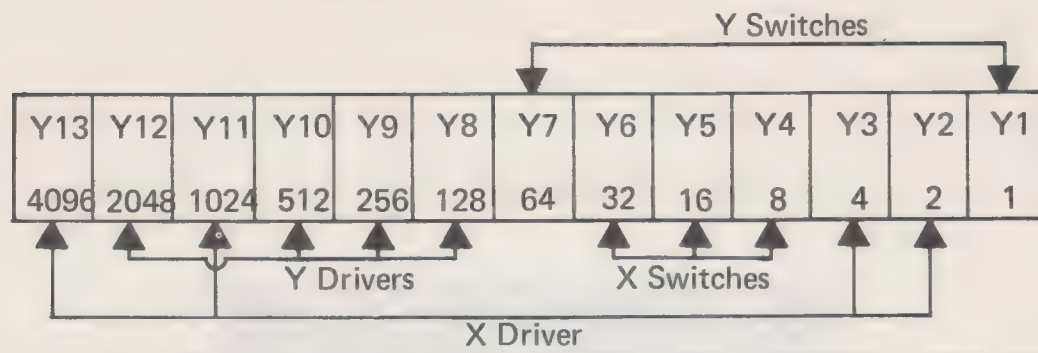


Figure 1

# MEMORY ADDRESS LATCHES



X DRIVERS							X SWITCHES						
Select Memory =	1	1	0				Select Memory =	1	1	0			
Select Memory Upper =	1	0	0				Select Memory Upper =	1	0	0			
Select Memory Special =	0	0	1				Select Memory Special =	0	0	1			
Y12	Y10	Y9	Y8				Y6	Y5	Y4				
0	0	0	0	X Dr 1	X Dr 1	X Dr 8	0	0	0	X Sw 1	X Sw 1	X Sw 8	
0	0	0	1	X Dr 2	X Dr 1	X Dr 8	0	0	1	X Sw 2	X Sw 2	X Sw 8	
0	0	1	0	X Dr 3	X Dr 1	X Dr 8	0	1	0	X Sw 3	X Sw 3	X Sw 8	
0	0	1	1	X Dr 4	X Dr 1	X Dr 8	0	1	1	X Sw 4	X Sw 4	X Sw 8	
0	1	0	0	X Dr 5	X Dr 1	X Dr 8	1	0	0	X Sw 5	X Sw 5	X Sw 8	
0	1	0	1	X Dr 6	X Dr 1	X Dr 8	1	0	1	X Sw 6	X Sw 6	X Sw 8	
0	1	1	0	X Dr 7	X Dr 1	X Dr 8	1	1	0	X Sw 7	X Sw 7	X Sw 8	
0	1	1	1	X Dr 8	X Dr 1	X Dr 8	1	1	1	X Sw 8	X Sw 8	X Sw 8	
1	0	0	0	X Dr 9	X Dr 1	X Dr 8							
1	0	0	1	X Dr 10	X Dr 1	X Dr 8							
1	0	1	0	X Dr 9	X Dr 1	X Dr 8							
1	0	1	1	X Dr 10	X Dr 1	X Dr 8							
1	1	0	0	X Dr 9	X Dr 1	X Dr 8							
1	1	0	1	X Dr 10	X Dr 1	X Dr 8							
1	1	1	0	X Dr 9	X Dr 1	X Dr 8							
1	1	1	1	X Dr 10	X Dr 1	X Dr 8							

Y DRIVERS							Y SWITCHES						
Select Memory =	1	1	0				Select Memory =	1	1	0			
Select Memory Upper =	1	0	0				Select Memory Upper =	1	0	0			
Select Memory Special =	0	0	1				Select Memory Special =	0	0	1			
Y13	Y11	Y3	Y2				Reg. Exp. Y7	Y1	Bit Ctr B				
0	0	0	0	Y Dr 1	Y Dr 1	B-Word Selects	0	0	0	Y Sw 1	Y Sw 1	Y Sw 3	
0	0	0	1	Y Dr 2	Y Dr 2	Y Dr 6	0	0	0	Y Sw 2	Y Sw 2	Y Sw 4	
0	0	1	0	Y Dr 3	Y Dr 3		0	0	1	Y Sw 2	Y Sw 1	Y Sw 3	
0	0	1	1	Y Dr 4	Y Dr 4		0	0	1	Y Sw 2	Y Sw 2	Y Sw 4	
0	1	0	0	Y Dr 5	Y Dr 1	A-Word Selects	0	1	0	Y Sw 3	Y Sw 1	Y Sw 3	
0	1	0	1	Y Dr 6	Y Dr 2	Y Dr 7	0	1	0	Y Sw 4	Y Sw 2	Y Sw 4	
0	1	1	0	Y Dr 7	Y Dr 3		0	1	0	Y Sw 4	Y Sw 1	Y Sw 3	
0	1	1	1	Y Dr 8	Y Dr 4		0	1	1	Y Sw 4	Y Sw 2	Y Sw 4	
1	0	0	0	Y Dr 9	Y Dr 1	Program Step Address Selects	1	0	0	Reg. Exp. & Sel. Mem. Upp. Are Not Used Together	Y Sw 3	Reg. Exp. & Sel. Mem. Sp. Are Not Used Together	
1	0	0	1	Y Dr 9	Y Dr 2	Y Dr 8	1	0	0	Y Sw 4	Y Sw 3	Y Sw 4	
1	0	1	0	Y Dr 9	Y Dr 3		1	0	1	Y Sw 3	Y Sw 4	Y Sw 3	
1	0	1	1	Y Dr 9	Y Dr 4		1	0	1	Y Sw 4	Y Sw 3	Y Sw 4	
1	1	0	0	Y Dr 9	Y Dr 1		1	1	0	Y Sw 3	Y Sw 4	Y Sw 3	
1	1	0	1	Y Dr 9	Y Dr 2		1	1	0	Y Sw 4	Y Sw 3	Y Sw 4	
1	1	1	0	Y Dr 9	Y Dr 3		1	1	1	Y Sw 3	Y Sw 4	Y Sw 3	
1	1	1	1	Y Dr 9	Y Dr 4		1	1	1	Y Sw 4	Y Sw 3	Y Sw 4	

Figure 2

## 23 K MEMORY

An Expanded Memory is now available for the MT/SC. This Memory has storage area above the PSAR, Register 2046.

Theoretically, the 23K Memory is divided into two sections: Upper and Lower Memory. The PSAR should be considered the Boundary between these two sections.

Basically, Lower Memory is the same as the 16K Memory. It contains Registers 0 through 2046, which includes the B-Word, the A-Word and the PSAR. These Registers are still addressed by using X Drivers 1 through 8, X Switches 1 through 8, Y Drivers 1 through 8 and Y Switches 1 through 4. The following signals are used in addressing Lower Memory in the same manner as they are used in addressing a 16K Memory:

- |                          |                  |
|--------------------------|------------------|
| 1. Select Memory         | 4. Select B-Word |
| 2. Select Memory Upper   | 5. Select A-Word |
| 3. Select Memory Special | 6. Select PSAR   |

In Order to address Registers in Upper Memory, it was necessary to include two additional X Drivers and one additional Y Driver. These are X Drivers Nine and Ten and Y Driver Nine.

Two Y Latches, Y12 and Y13 have been added to select these additional Drivers. Y13 is used to select Y Driver Nine. Y12 is used to select X Driver Nine. Y12 and Y8 are used to select X Driver Ten. Of course, there are other signals involved, such as Select Memory Upper, but this should explain the Y's involved.

The Chart in Figure 2 shows the relationship between the Y Latches and the Switches and Drivers.

The 23K Memory contains 2,880 bytes. Normally, the binary total of the Y Latches that are on determines the byte that will be addressed by those Y Latches. The number of addresses that can be derived from the possible combinations of 13Y Latches far exceeds 2,880. Because of this, an address can be calculated for a byte that doesn't exist. Every combination of Y Latches will address some byte in Memory, but in Upper Memory this byte cannot always be identified by adding up the binary value of the Y Latches that are on.

Notice on the Chart (Figure 2) that Y13 will select Y Driver 9, regardless of the condition of Y's 2, 3 & 11. This means, if Y13 is being used, Y's 2, 3 & 11 should not be added into the binary total, even if they are on. This also means that those bytes whose address would be derived by adding up combinations of Y13 with Y's 2, 3 & 11 do NOT even exist.

The same is true of Y12 where Y's 9 and 10 are concerned. The following example will illustrate this point:

$Y13 \& Y12 = \text{Binary } 6144 = \text{Address of byte } 6144.$

$Y13+Y12+Y11+Y10+Y9+Y3+Y2 = \text{Binary } 7942 = \text{Address of byte } 6144.$

If Y13 is used without Y12, then Y's 9 & 10 should be added into the total if they are on.

If Y12 is used without Y13, then Y's 2, 3 & 11 should be added into the total if they are on.

## USE OF UPPER MEMORY

The bytes in Upper Memory involve the use of Y12 and/or Y13 in their address. The conditions under which these Y Latches can be set dictates what the bytes in Upper Memory can be used for.

Y12 is the only one of the two that can be set during I-O (see ILD's). This means that bytes (Registers) which can be addressed by combinations of Y Latches, including Y12, can be used as Program Step Registers.

Y12 can also be set during I-2 time, but this serves no purpose since Select Memory Upper will be down during any Instruction Time that directly follows I-2 time.

Y12 and/or Y13 can be set during I-4 or I-8 time. This means that bytes which can be addressed by combinations of Y Latches, including Y12 and/or Y13 can be used as the Indirect byte in Indirect Arithmetic (see "Instruction Set Data Flow", page 13-23 of the Instruction Manual).

These Bytes CANNOT be used in Multiplex Output because they do not run consecutively.

Refer to ILD, page 320, for the Logic involved in setting Y12 and Y13.

## BOUNDARY JUMP

As mentioned before, the PSAR should be considered the Boundary between Upper and Lower Memory.

With a 23K Memory, part of the Program Steps may be in Upper Memory and the remainder in Lower Memory.

The Normal Jump Program Steps can be used to alter the consecutive routine of the Program while in either area of Memory, but they CANNOT be used to jump from one area to the other (i.e., cannot Jump from PS 560 to PS 2050).

The Program Step necessary to Jump from a Program Step on one side of the Boundary to a Program Step on the other side is called a Boundary Jump.

If a Boundary Jump is performed while in Lower Memory (not using Y12), a Flip Latch called "Select Y12" will set. The Boundary Jump PS will contain the Address, excluding Y12, of the PS in Upper Memory to be performed next. The "Select Y12" Signal will cause Y12 to set during all the following I-O times until the next Boundary Jump PS is performed. This will cause Y12 to be included with the Address in PSAR.

*Example:* The PSAR contains a binary 2. This  $2+Y12(2048) = \text{The Address of the PS is } 2050.$

If a Boundary Jump PS is performed while working in Upper Memory (using Y12), the "Select Y12" Flip Latch will reset and remain off until the next Boundary Jump PS is performed.

*NOTE:* An Indirect Arithmetic PS from either Upper or Lower Memory can work with bytes in Upper Memory.

This is the Program Step Set for the Boundary Jump PS's:

op 1	op 2	op 3	op 4	op 5	Address op 6	op 7	
0	0	0	0	1	1024	512	UNCONDITIONAL
0	0	0	1	1			JUMP ON HIGH
0	0	1	0	1			JUMP ON LOW
0	0	1	0	1			JUMP ON EQUAL
0	0	1	1	1			JUMP ON NOT EQUAL

As shown by this chart, a Boundary Jump can be either Unconditional or Conditional. It may be noticed that these are the same Program Steps known to a 16K Memory as Conditional Jumps with Link. The only Jump with Link Program Step that will be honored by the 23K Circuitry is an Unconditional Jump with Link.

#### PURPOSE:

The Boundary Jump PS is performed to accomplish two things:

1. To condition the "Select Y12" Flip Latch to correspond with the direction jumped across the Boundary.
2. To change the Value in the PSAR so it will contain the Address of the Program Step that is to follow the Boundary Jump PS (excluding Y12).

The Logic of the Boundary Jump PS is as follows:

#### I-0 Where is the Program Step?

This is like all other I-0 Times. Its purpose is to read the PSAR, load the Y Latches to the Address of the Program Step, bump this value by two and write it back into the PSAR.

#### I-1 What is the Program Step?

This is like all other I-1 Times. Its purpose is to read the PS Register, duplicate the PS in the A-Word, load the Operational Code Latches to define the PS, and preserve the PS by writing it back into the PS Register.

#### CONCLUSION OF I-1 TIME:

The signal "Jump" should be up to define the Operation.

If the conditions of the PS are met — unconditional, low, high, equal or not equal — the "Taken" Signal will be up. (If the conditions are NOT met, "Taken" will be down and the clock will Permute back to I-0 time and perform the next PS.)

"Jump" and "Taken" along with other Signals will bring up the Signal "Boundary Jump".

"Boundary Jump" and "Upset Preinhibit" (I-1, B 13-16) will "and" with either state of the Y12 Latch to condition the "Select Y12" Latch. If the Y12 Latch is off during I-1 time, "Select Y12" will set. If the Y12 Latch is on during I-1 time, "Select Y12" will reset.

"Boundary Jump" will bring up "Set 9" which will cause the clock to permute to I-9 time.

I-9 Transfer the Address in the A-Word to the PSAR

The Address of the next PS, excluding Y12 if it is in

Upper Memory, is in the A-Word. During I-9 time, this Address, along with the Bits that loaded the Operational Code Latches, is transferred to the PSAR.

AT THE END OF I-9 TIME THE CLOCK WILL PERMUTE BACK TO I-0 TIME.

#### REGISTER EXPAND

This is a feature of the 23K Memory and its circuitry. Register Expand increases the working (low order) registers by the value of 64. In other words, if you did a Program Step to Output from Register 4 and used the Register Expand capabilities, the machine would actually output from Reg. 68 (4 plus 64 equals 68).

A Program Step that utilizes the Register Expand feature must be preceded by a Prefix Program Step. This Prefix PS sets up a condition so that the value of 64 can be added to the Low Order Address in the FOLLOWING Program Step. In the case of Direct or Indirect Arithmetic, 64 can be added to either or both Low Order Addresses. The Prefix PS determines which.

#### PREFIX PROGRAM STEP

A prefix PS can be used to Expand the Address in the following PS:

1. All Arithmetic Operations.
2. All Immediate Arithmetic Operations.
3. All Program Control Operations.
4. Input and Output (except Multiplex).

*NOTE: The Prefix PS applies only to the PS immediately following it.*

This is the Program Step Set for the Prefix Step:

op1	op2	op3	op4	op5	op6	op7
1	0	Px A2	Px A1	0	0	1

This Program Step runs: I-0, I-1, I-2, and I-3.

#### PURPOSE:

The Prefix PS is used to condition the Prefix Address One and Prefix Address Two Flip Latches.

These Latches, if set, will NOT be used until the following Program Step.

#### I-0 Where is the (Prefix) Program Step?

This is like all other I-0 times.

#### I-1 What is the Program Step?

This is like all other I-1 times.

Loading Operational Codes 1 & 7 causes the Signal, "Prefix" to come up.

I-2 Read the A-Word and Write It Back.

*NOTE: Y1 & Y5 will Load but they are insignificant to this PS.*

If Operational Code 3 is ON, Prefix Address 2 will SET.  
If Operational Code 4 is ON, Prefix Address 1 will SET.

I-3 Read out a Memory Location & Write It Back.

*NOTE: The only purpose in going through I-3 time is because the Clock cannot be Permuted to I-0 from I-2 with existing logic. Reading out the Memory Location and writing it back during I-3 time is a redundant operation. The Memory Location will be Register 16 (Y5) or Register 80 (Y5 and PX A1).*

At the end of I-3 time: Inst. T. 3, -Opl C 2, -Input, -Output and -MR will cause the Clock to Permute to I-0 time (refer ILD, page 0304 in Section 13 of the Instruction Manual).

#### REGISTER EXPAND FLIP LATCH

This Latch, when set, does exactly the same thing that Y7 (and Select Memory Upper) does (see Fig. 2). Since the binary value of Y7 is 64, the binary value of the Register Expand Latch is 64. Both Signals go to an "or" block; therefore, the value should not be doubled if they are both on.

The Register Expand Latch can only be set during I-2 and I-6 time.

If Prefix Address One was set by a preceding Prefix PS, Register Expand will set during I-2 Time. This will add 64 to the Address being set in the Y Latches at this time.

*NOTE: Select Memory Upper will ALWAYS be down during the Instruction Time following I-2; therefore, only Y2 through Y6 and Register Expand should be considered in calculating the Address.*

Register Expand will be reset when the Y Latches are reset.

If Prefix Address Two was set by a preceding Prefix PS, Register Expand will set during I-6 time. This will add 64 to the Address being set in the Y Latches at this time. Again, Register Expand will be reset when the Y Latches are reset.

The Prefix Program Step must DIRECTLY precede the Program Step in which Prefix Address One and/or Prefix Address Two are to be used.

During the Program Step following the Prefix PS, Prefix Address One will be reset, if it is on the first time the Clock Permutes. It is used during I-2 time. The normal stepping of the Clock; I-0, I-1, and I-2 will Not reset it.

Prefix Address Two will reset, if it is on when the Clock Permutes from an I-time using Instruction Time Counter "D" (binary 8). Since it is used during I-6 time, this will be when the Clock Permutes from I-9 to I-0.

Refer to ILD, page 321, for the Logic involved in Register Expand.

